BEOL-Compatible On-Chip DC-DC Converters

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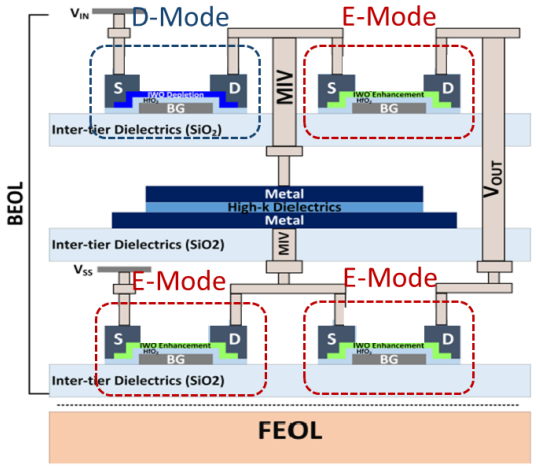
Outline of Presentation



Power Delivery Challenges in Heterogenous 3D (H3D) Integrated Circuits

High-Efficiency On-Chip DC-DC Voltage Converters

Back-End-of-Line Compatible On-Chip Components

- Amorphous Oxide Semiconductor (AOS) Power Transistors
- Enhancement- and Depletion-Mode AOS Power Transistors
- High-Density Capacitors with High Breakdown Voltage

On-Chip DC-DC Converter Performance

Summary

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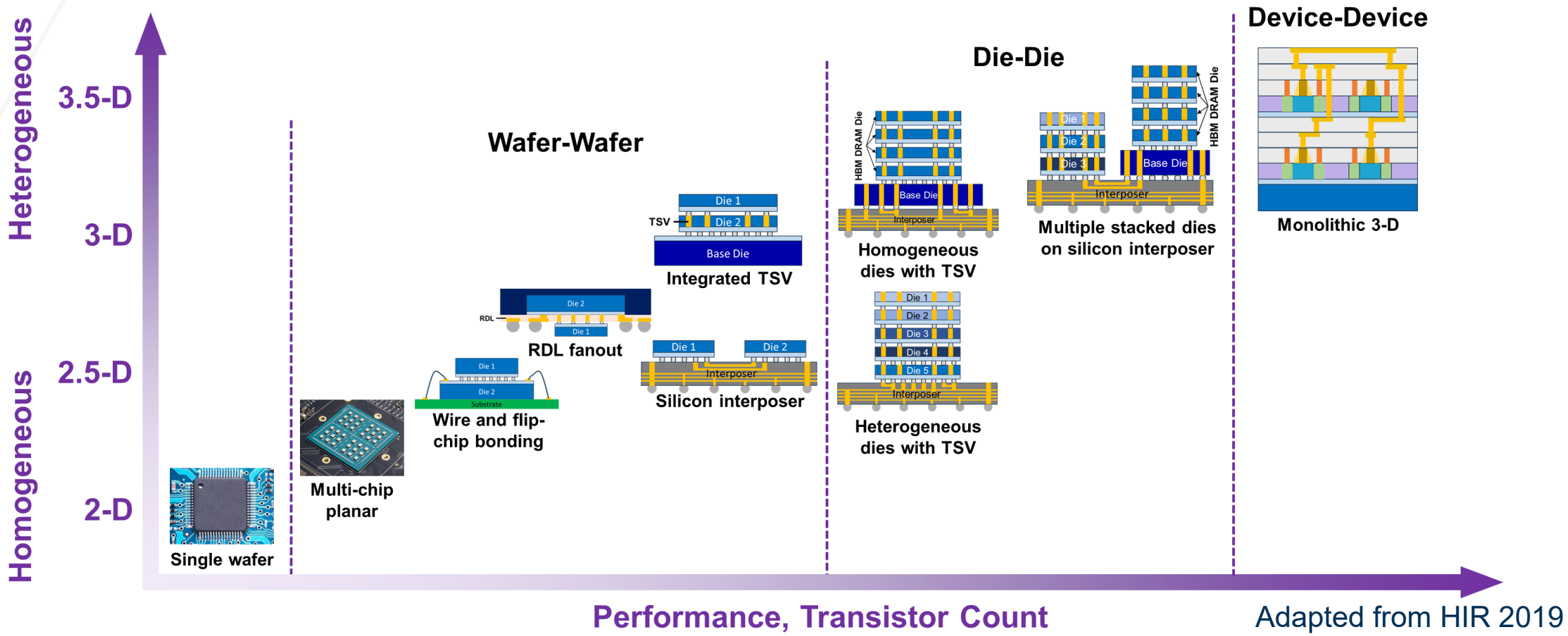
Heterogenous Integrated Circuits



- With a variety of chiplets seamlessly integrated, heterogenous ICs enable system performance scaling.

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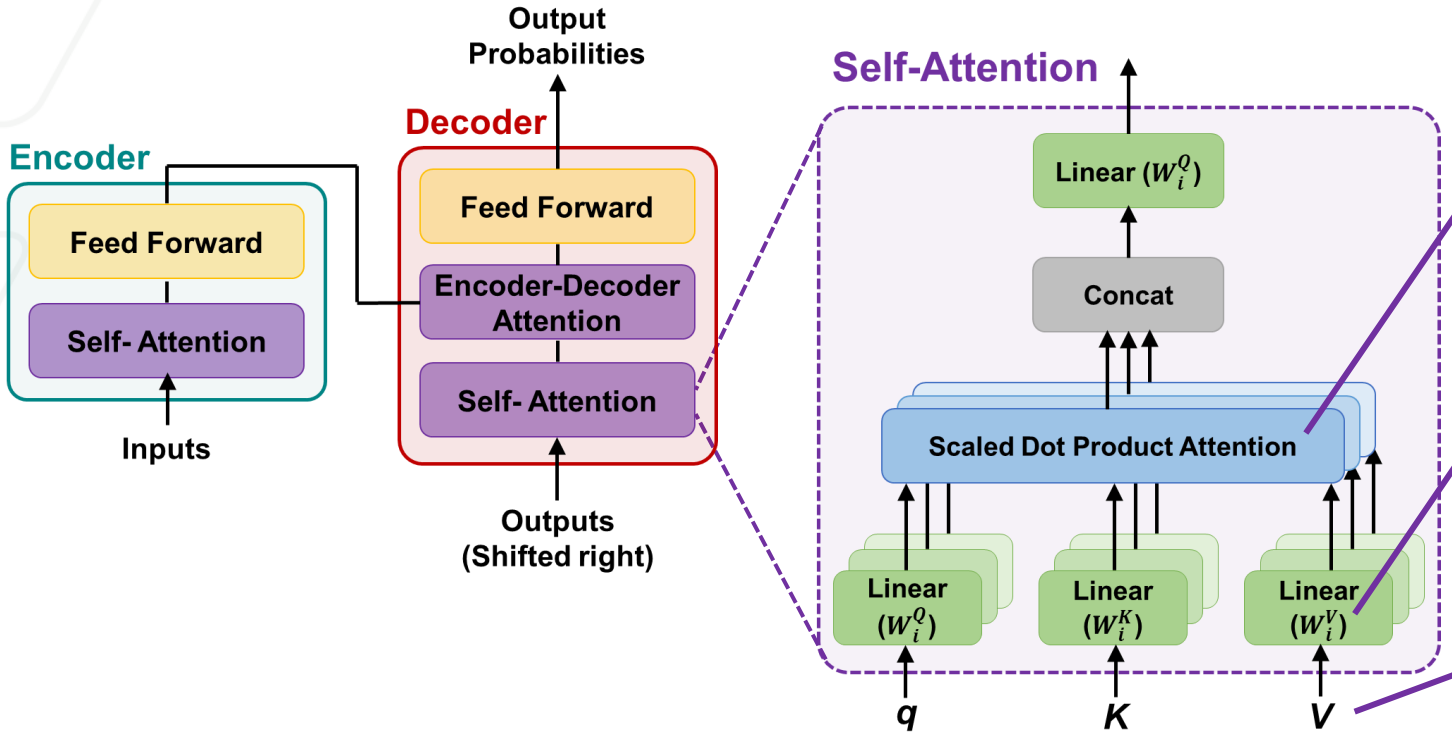
Example: Transformer Accelerator

Transformer architecture



176B 280B 340B 1.085T 1.7T

# of model parameters

Technology mapping

- Compute unit
  (for attention, feedforward, etc.)
  - Leading-edge logic node
- Weight memory
  (for pre-trained weight storage)
  - Infrequent write operations
  - Non-volatile memory
- Global buffer
  (for attentional caches, etc.)
  - Frequent write operations
  - Lower write time & energy
  - Higher endurance
  - Higher memory density

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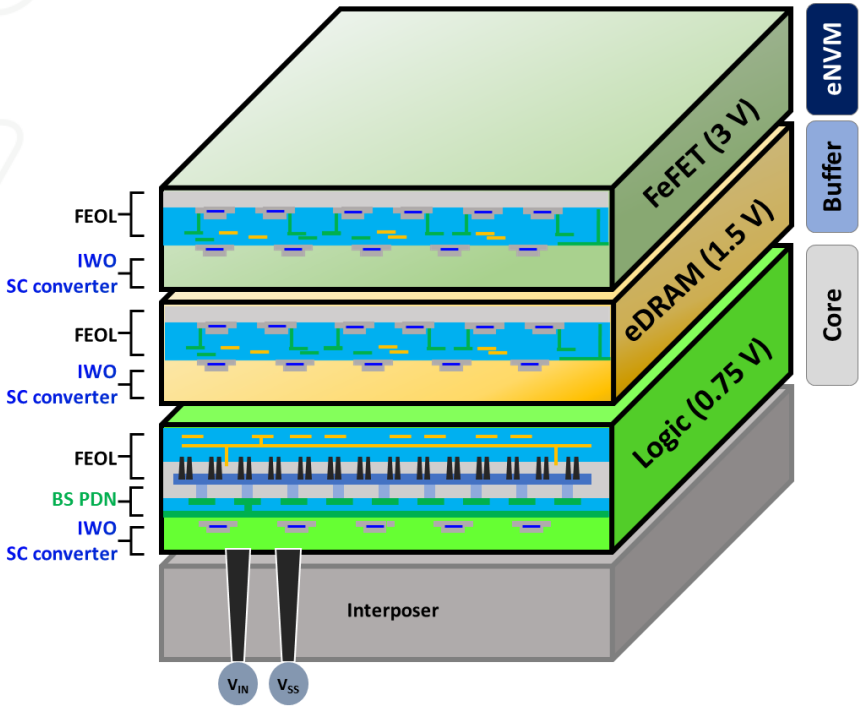
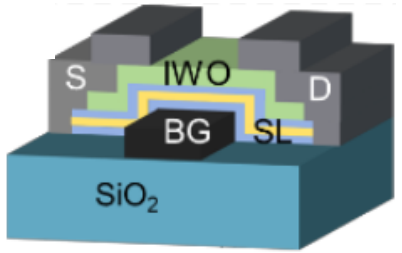
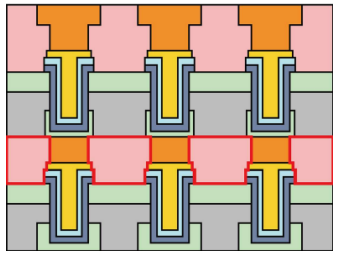
Multiple Voltage Domains in Heterogenous ICs

Multi-Tier Stacked Transformer Accelerator

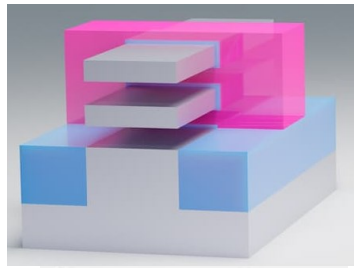




IWO FeFET
- Weight memory
- 22 nm node



2T0C eDRAM
- Global buffer
- 7 nm node



Nanosheet FET
- Compute unit
- 2 nm node

➢ In heterogenous ICs, different functional tiers may adopt various technology nodes, requiring multiple voltage domains.

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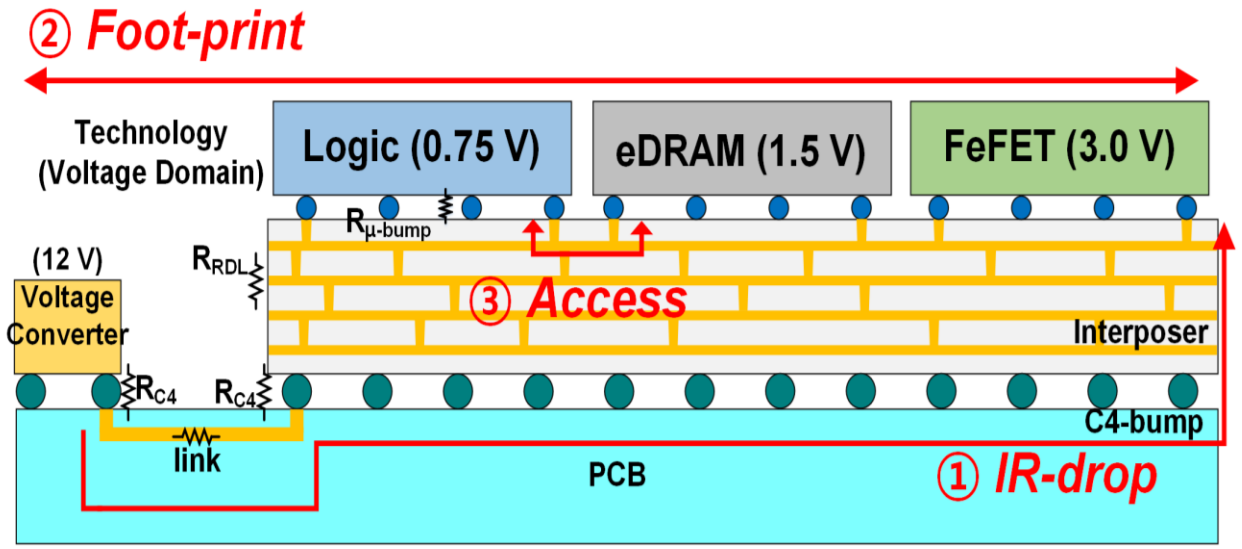
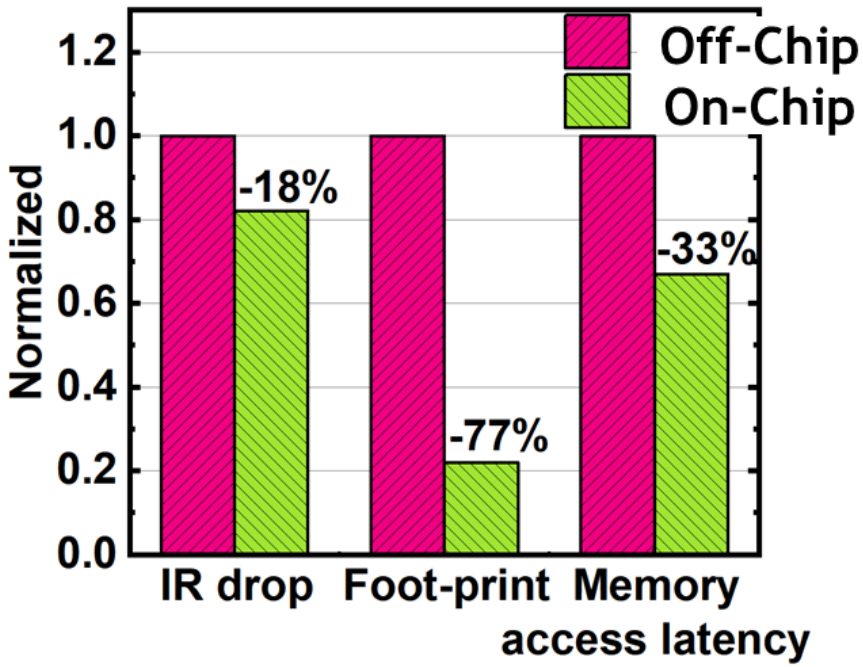
Power Delivery Challenges in Heterogenous ICs

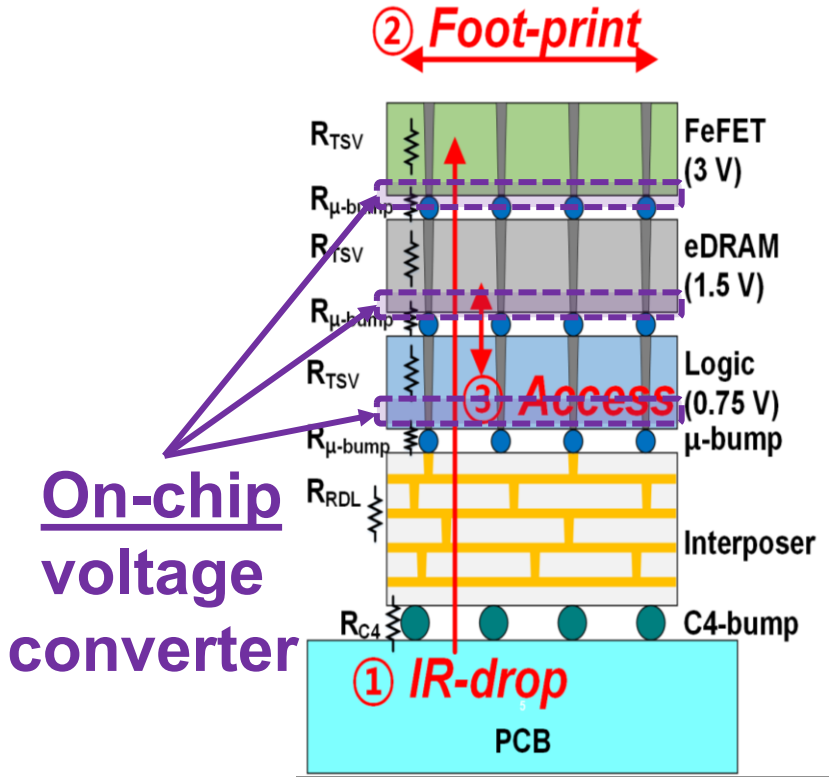


In heterogenous ICs (with **multiple supply voltage domains**):

- ❖ Increased power density demands cause >10% IR drops and routing losses
- ❖ Off-chip voltage converters increase package footprint
- ❖ Long inter-tier signal length (>100 μm) rises data access latency

H3D ICs with On-Chip Voltage Converters





- Heterogenous 3D (H3D) architecture with on-chip voltage converters (at least from input 12V to 0.75V) in each tier provides a reduction in IR drop, area, and memory access latency.

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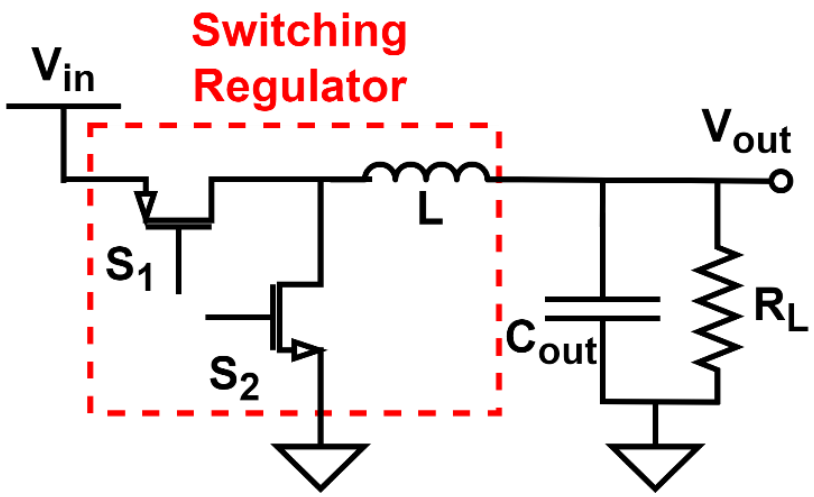
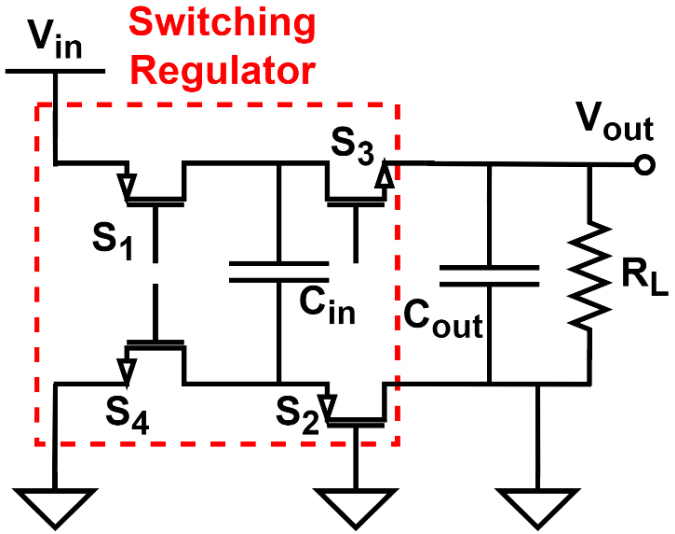
On-chip DC-DC Converter Options

Switched-Inductor



- Pros: high efficiency across a wide range of output voltages (off-chip)
- Cons: large area
  increased fab cost & complexity
  degraded performance (on-chip)

Switched-Capacitor (SC)



- Pros: CMOS Compatible
  Lower intrinsic loss
- Cons: Efficiency vs. conversion ratio (determined by topology)

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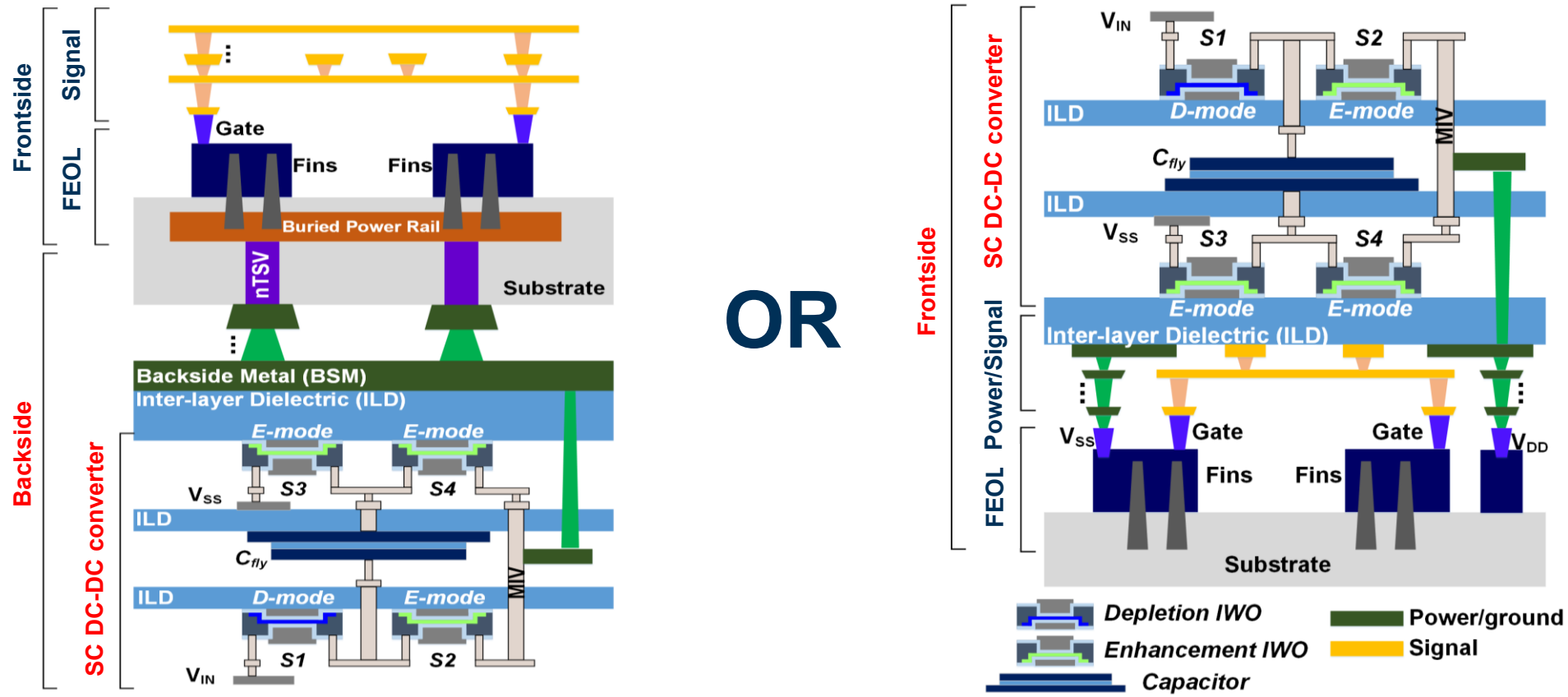
Feasible M3D Integration for SC DC-DC Converters



- Monolithic 3D (M3D) integration can further improve power density and area efficiency of SC DC-DC converters in either backside or frontside BEOL.

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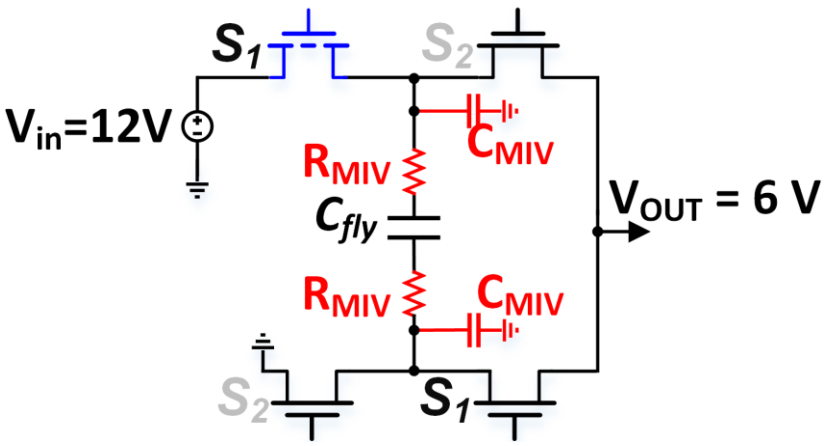
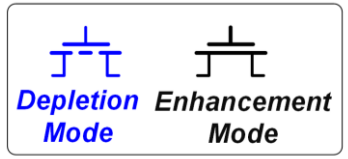
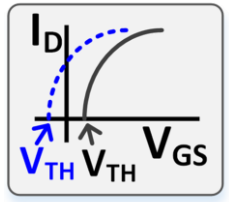
Technology Requirement







Category	Parameter	Target
On-chip SC DC-DC converters	Voltage conversion	12 V to 6 V
	Power density	1 W/mm^2
	peak efficiency	84%
BEOL-compatible power FETs	On-resistance	14 mΩ·mm^2
	Breakdown	>12 V
	Switching freq.	100 MHz
	Enhancement & depletion mode?	Yes
BEOL-compatible flying capacitors	Breakdown	>6 V
	Capacitance density	400 fF/um^2
	Leakage density	50 pA/mm^2

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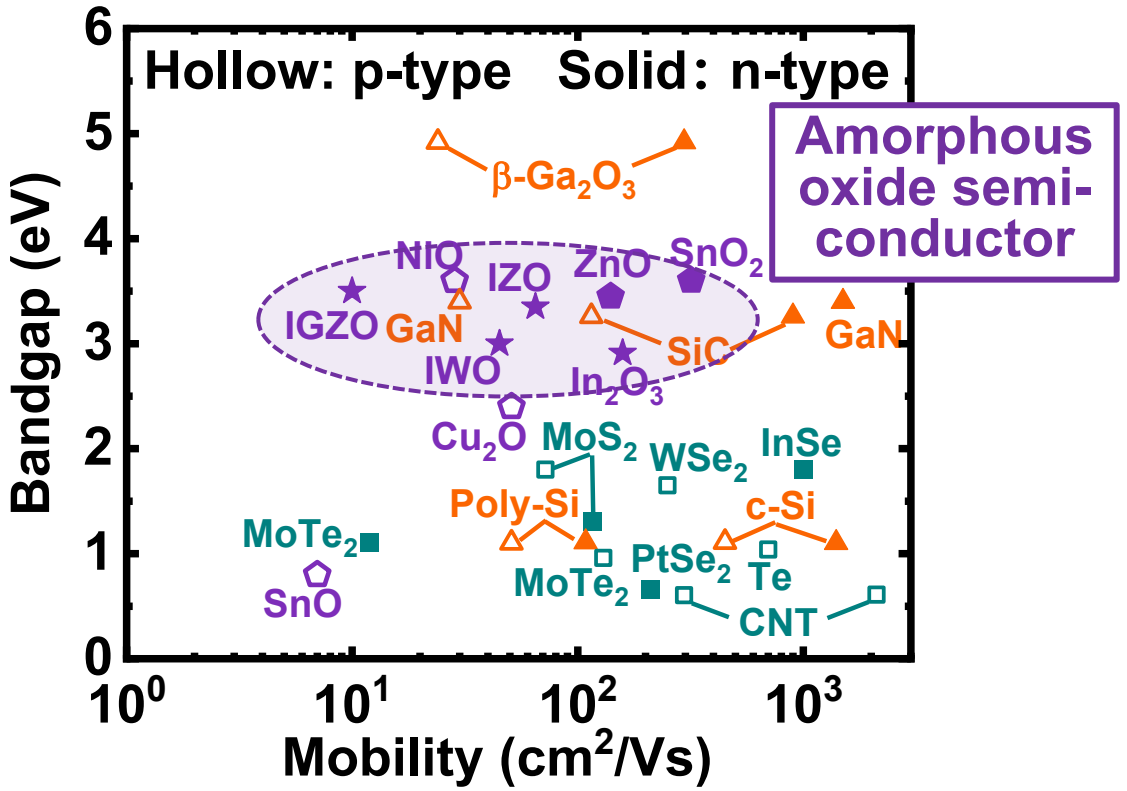
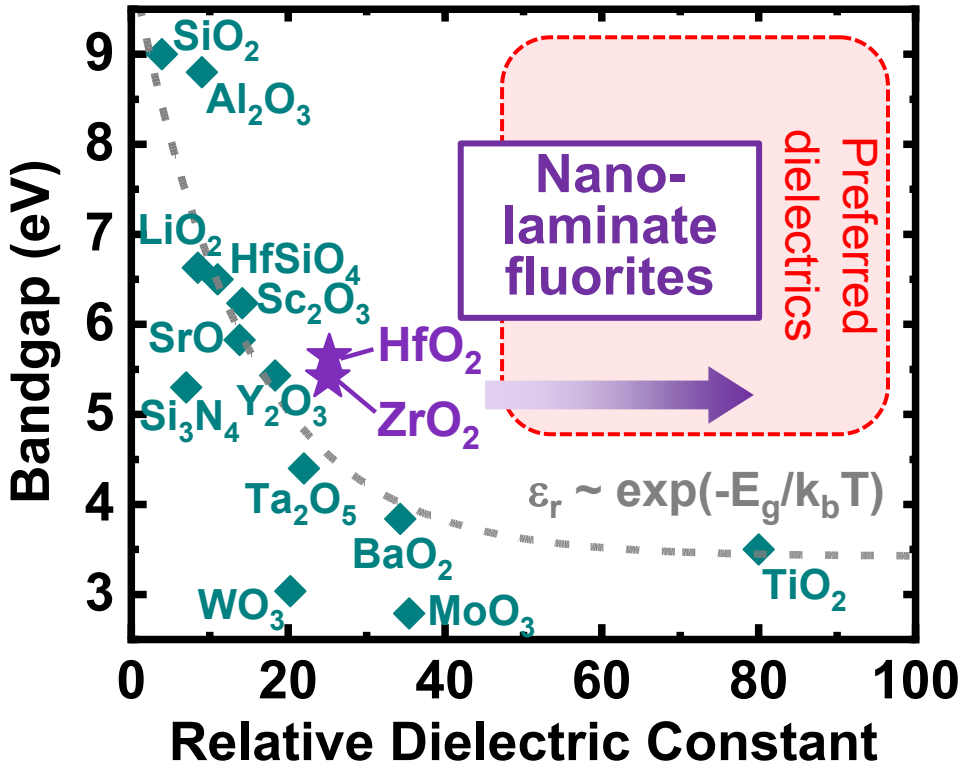
Materials Candidates for Device Components at BEOL

Power FETs at BEOL



Flying Capacitors at BEOL



- Amorphous oxide semiconductors for power switches and nanolaminate fluorites for flying capacitors are promising candidates.

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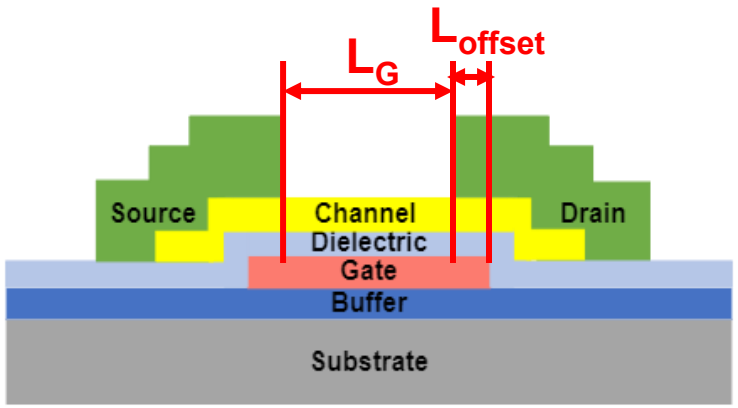
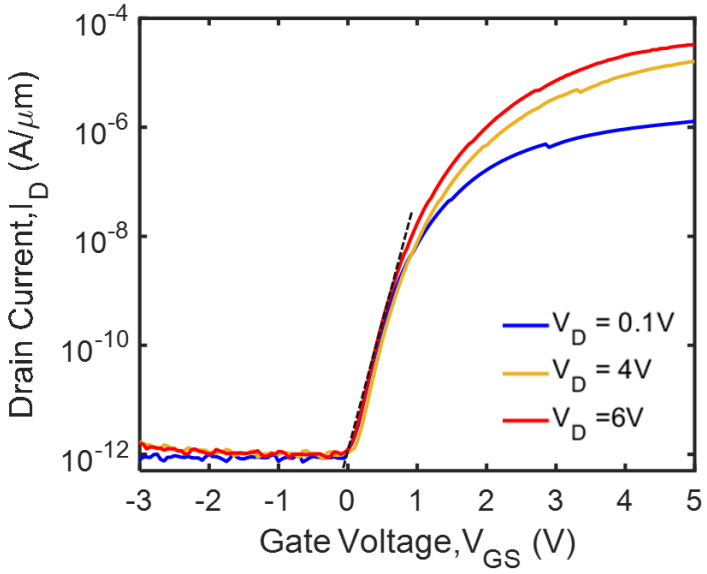
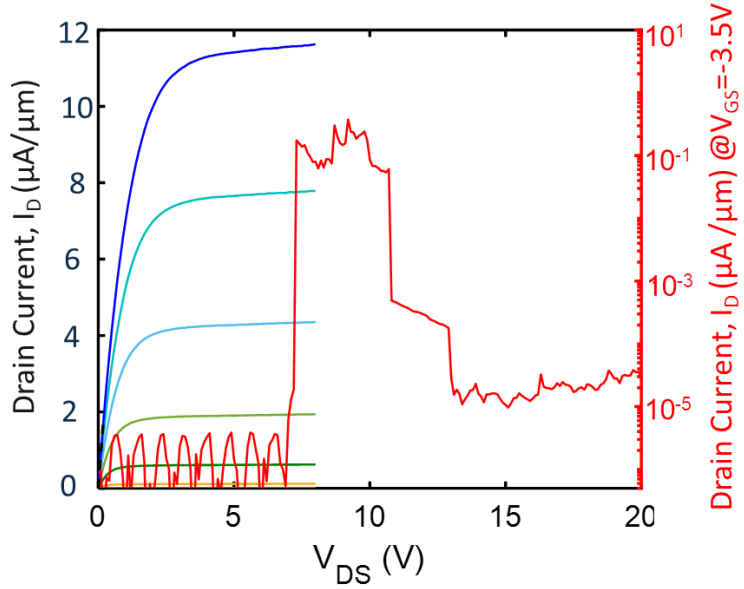
IWO MOSFET with G-D Overlap (Conventional)

Conventional FET with G-D Overlap



W/L_G = 10 μm/500 nm, L_{offset} = -300 nm





- Device fabrication max temperature is below 300°C.
- Off-state drain breakdown voltage (V_{BD}) in the conventional IWO FETs with G-D overlap is ~7 V.

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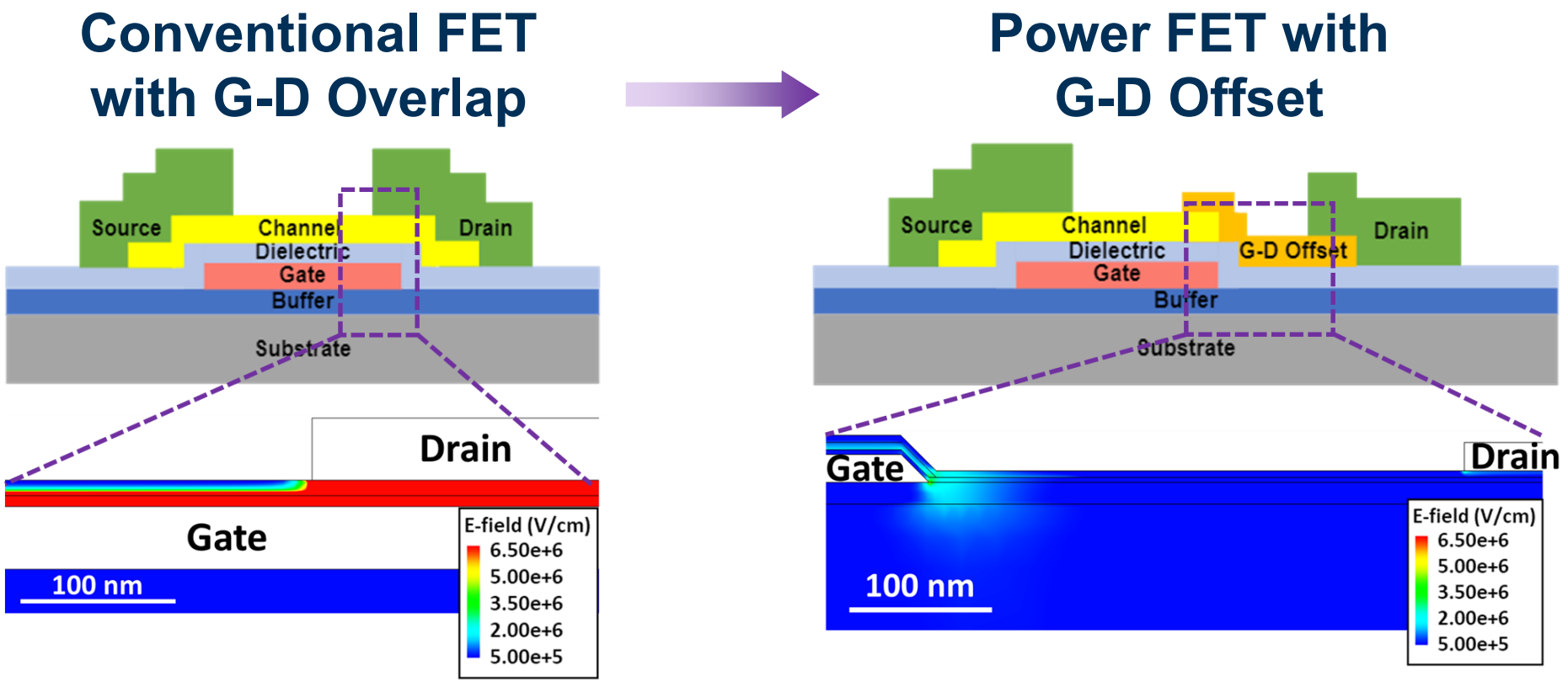
IWO Power FETs with G-D Offset



- Peak electric field along channel length is reduced by 12.7x in the power FETs with G-D offset compared to the conventional MOSFETs.

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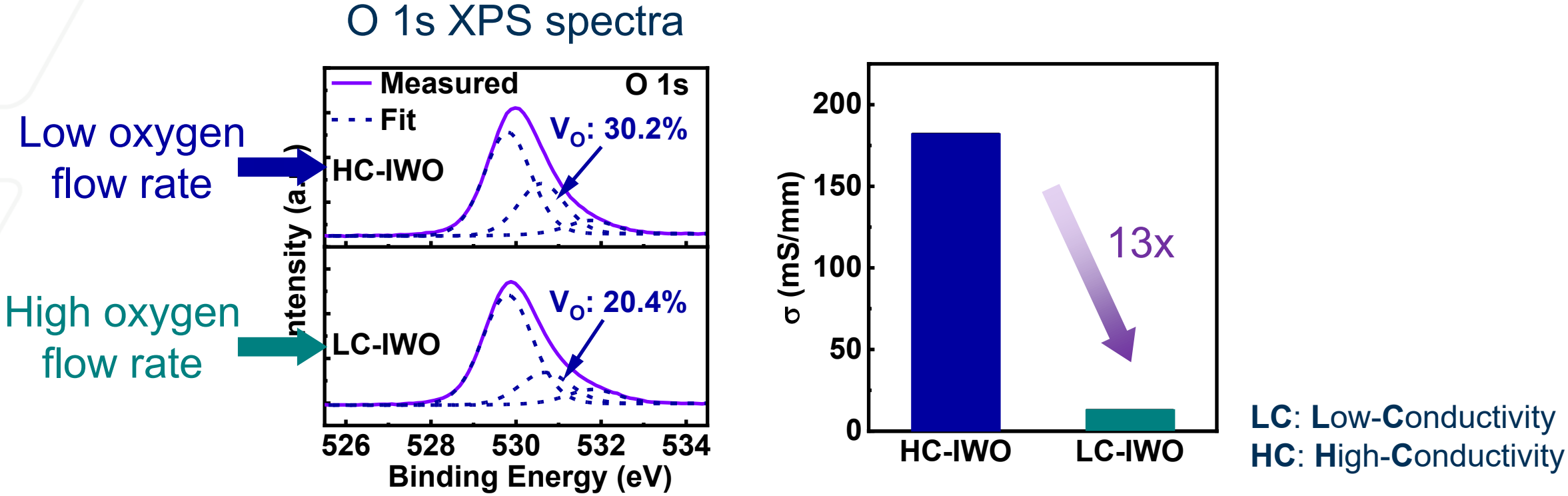
IWO Conductivity Modulation for E- & D-mode Power FETs



- Key strategy: IWO conductivity (and device V_{TH}) can be modulated by oxygen flow rate in IWO deposition.

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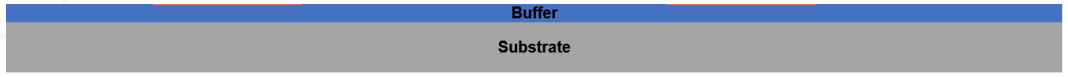
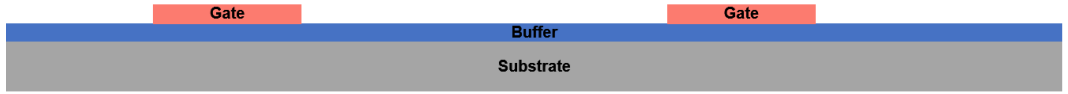
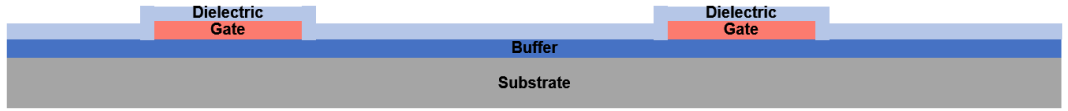
E- & D-mode IWO Power FET Process Flow



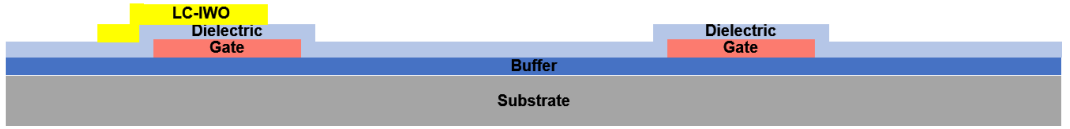
1. Buffer layer (90 nm SiO_2 + 15 nm HfO_2) dep.



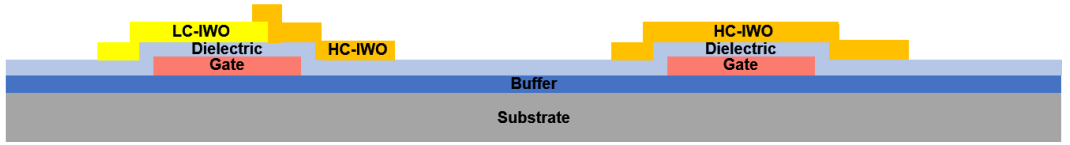
2. Gate electrode (25 nm Pd) dep. & pat.



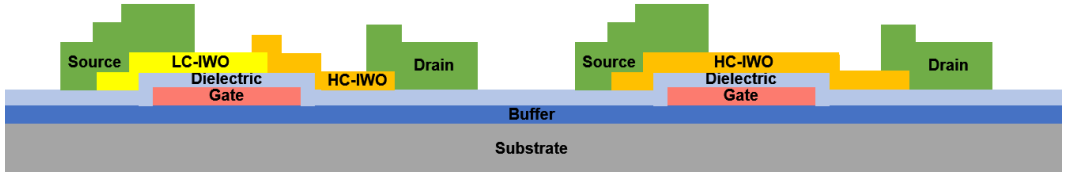
3. Gate insulator (35 nm HfO_2, PEALD, 250 ℃) dep.



4. **LC-IWO** dep. & pat. for **E-mode channel** (5 nm, 6 sccm O_2 for sputtering)



5. **HC-IWO** dep. & pat. for **D-mode channel** & **offset region** (8 nm, 0.6 sccm O_2 for sputtering)



6. Source/drain contact (40 nm Pd) dep. & pat.

➢ Process temperature remains below 300°C.

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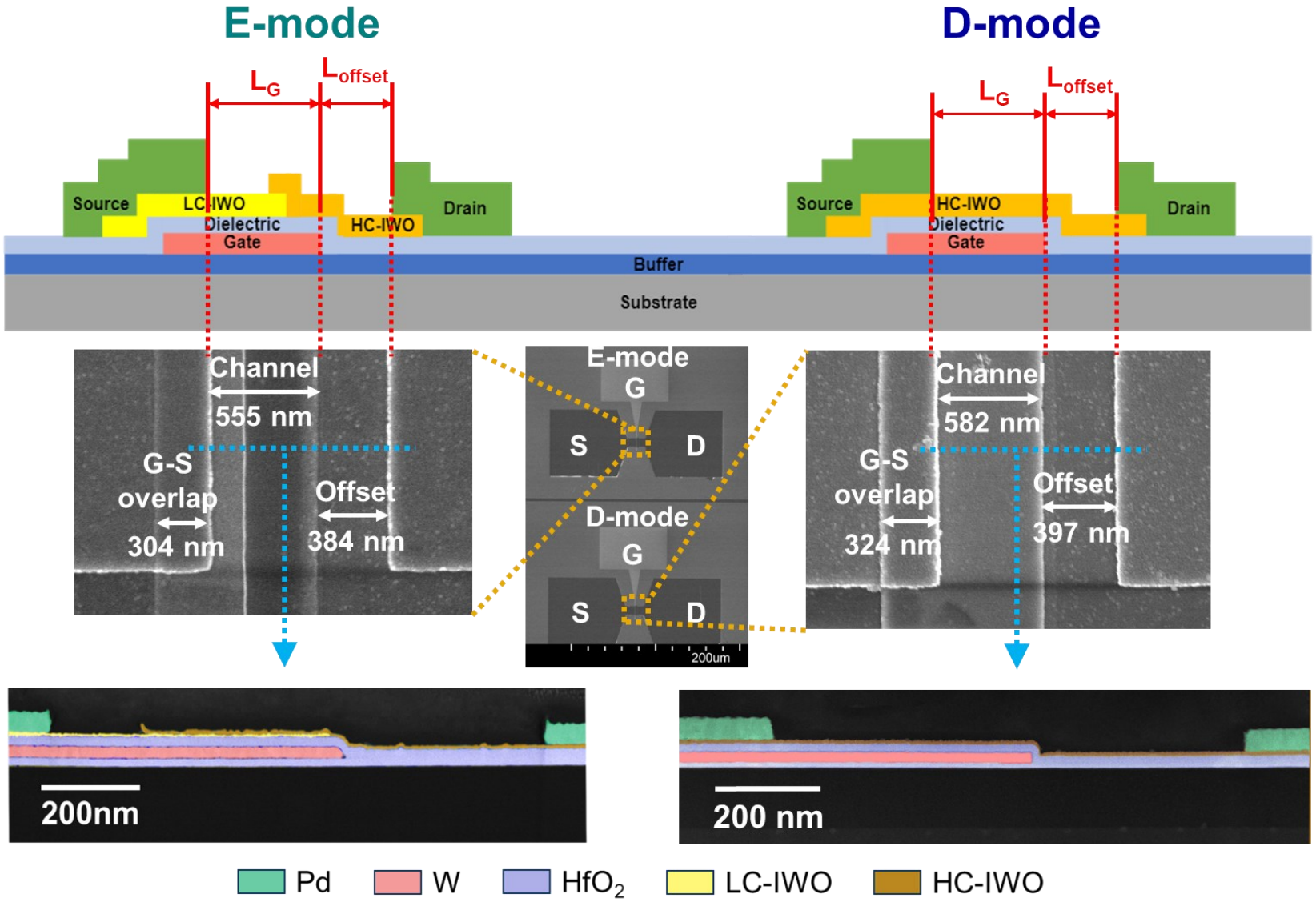
E- & D-mode IWO Power FET Co-integration



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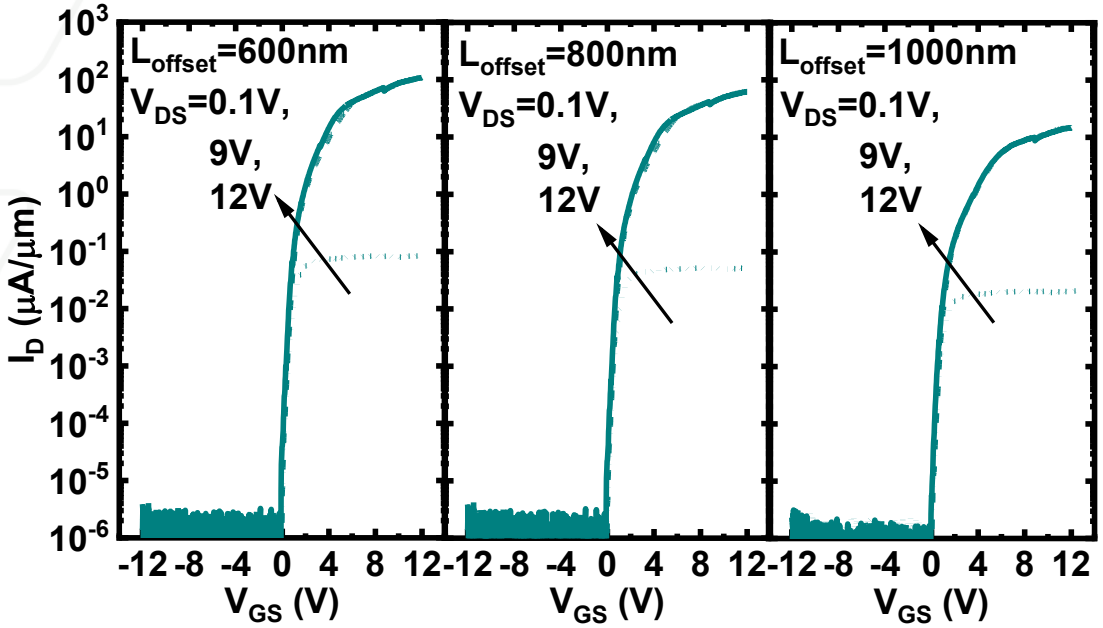
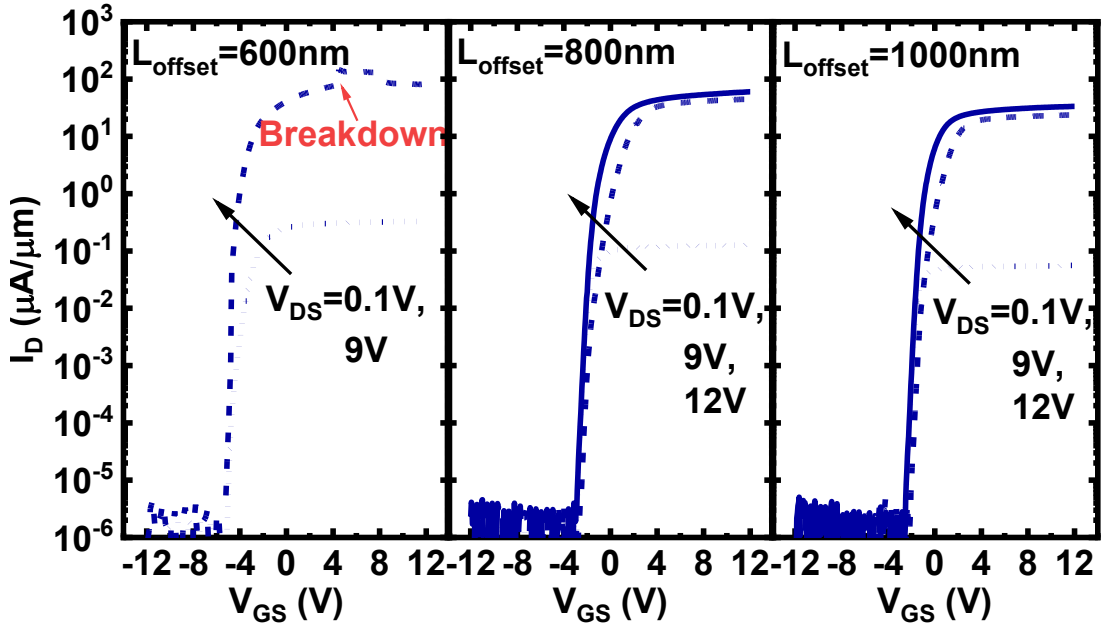
Transfer Characteristics

E-mode (L_G = 600 nm)



D-mode (L_G = 600 nm)



- The E-mode power FETs have a positive V_{TH} (=1.1 V @L_{offset} = 800 nm) and the D-mode power FETs show a negative V_{TH} (=-1.7 V @L_{offset} = 800 nm).

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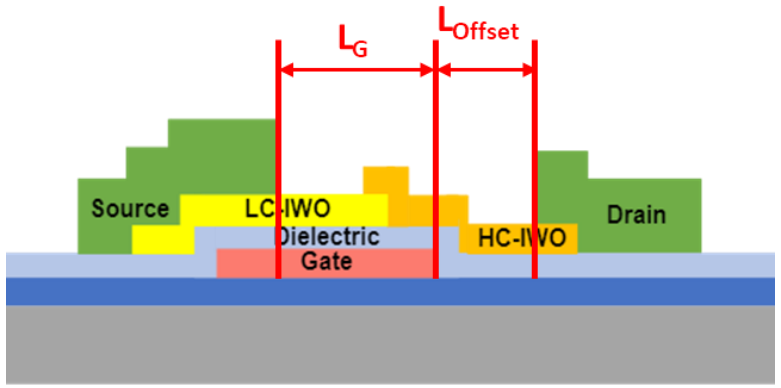
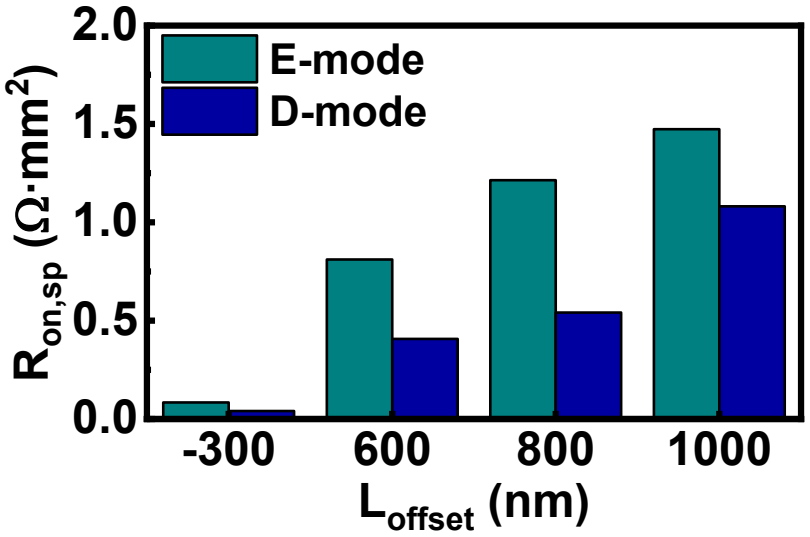
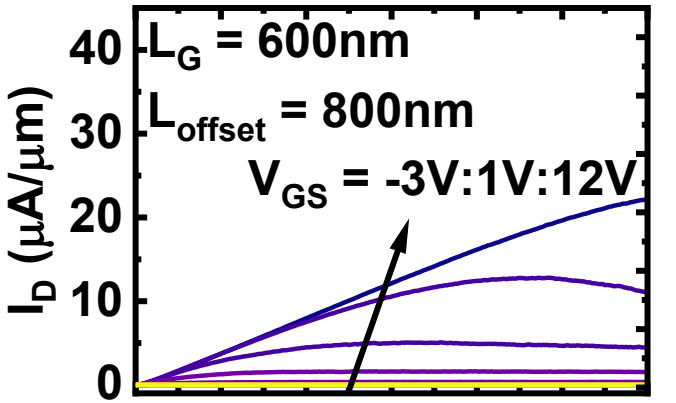
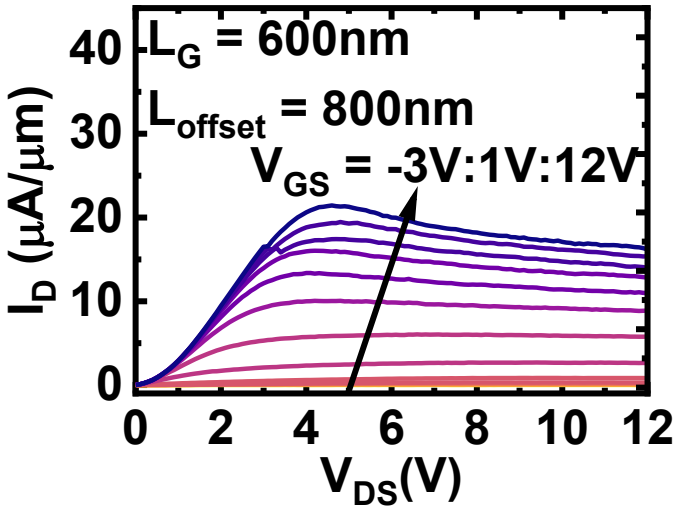
Specific On-Resistance







E-mode



D-mode

- The power FETs show >10x larger $R_{on,sp}$ than the conventional MOSFETs.
- 1.7x increase in L_{offset} leads to 1.8x (E) and 2.6x (D) increase in $R_{on,sp}$.

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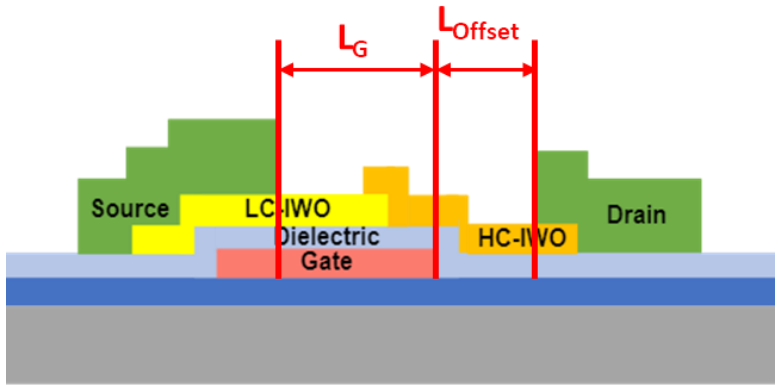
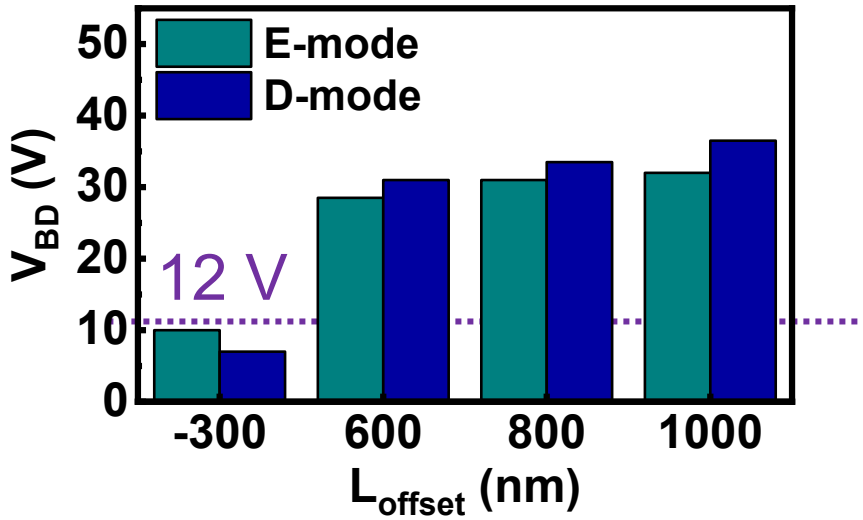
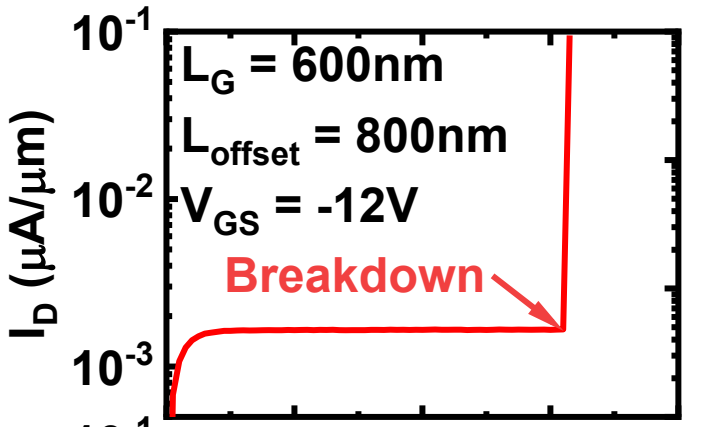
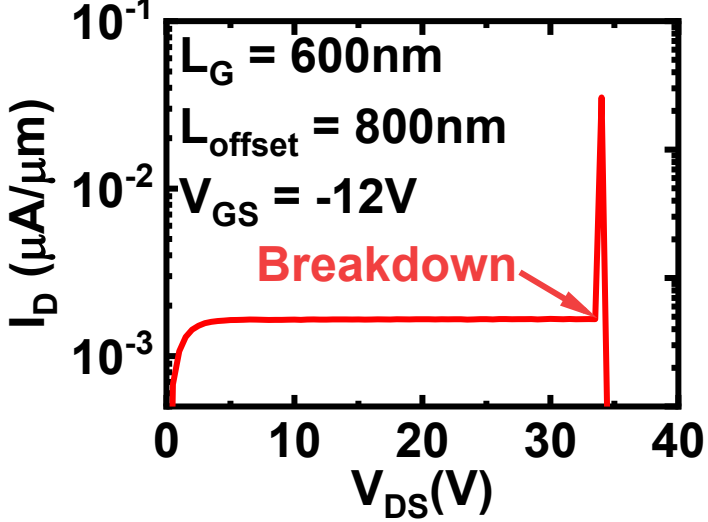
Drain Breakdown Voltage







E-mode



D-mode

- The power FETs show a off-state drain V_{BD} of >12 V, which is >3x higher than the conventional MOSFETs.
- Tradeoff: 3-4x increase in V_{BD} for ~14x increase in $R_{on,sp.}$

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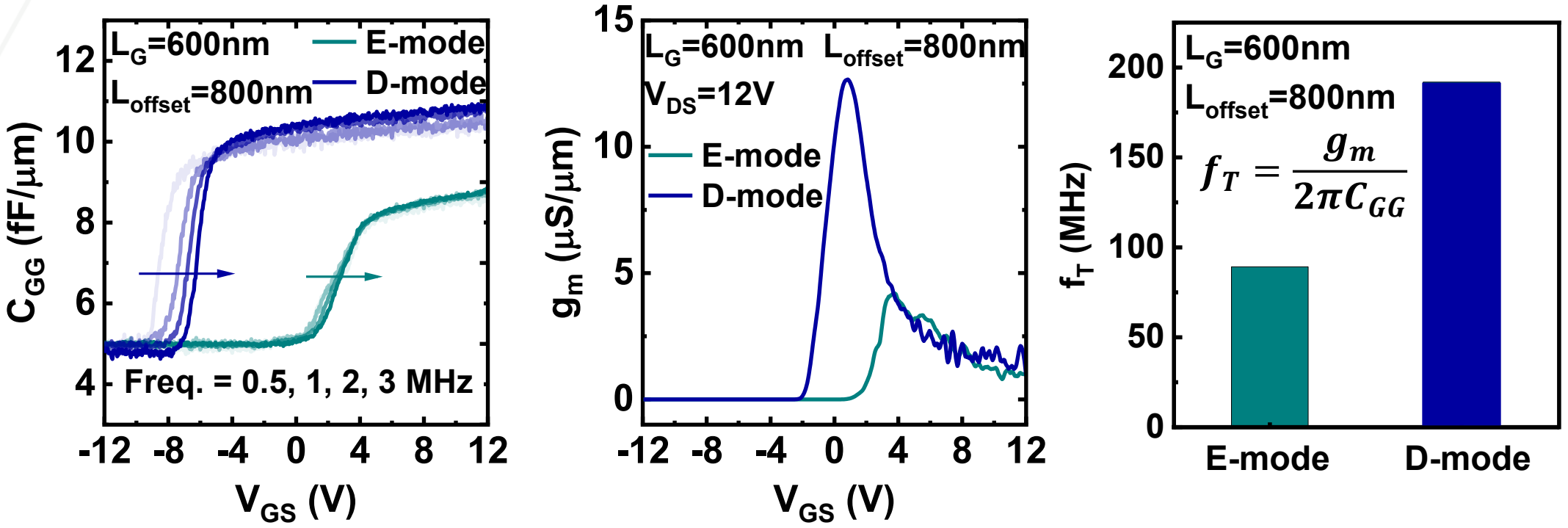
Switching Characteristics



- E- and D-mode devices (L_{offset} = 800 nm) exhibit an estimated switching frequency f_T of 90 MHz and 192 MHz, respectively.

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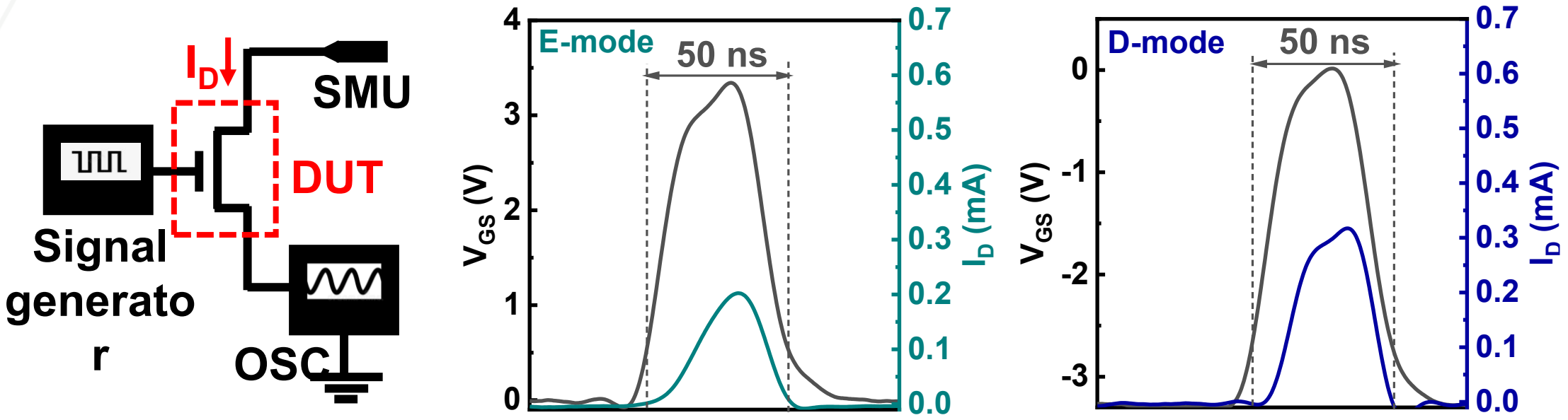
Pulse Response



- Both devices (at V_{DS}=12 V) can respond to the 50-ns-wide input gate pulses.

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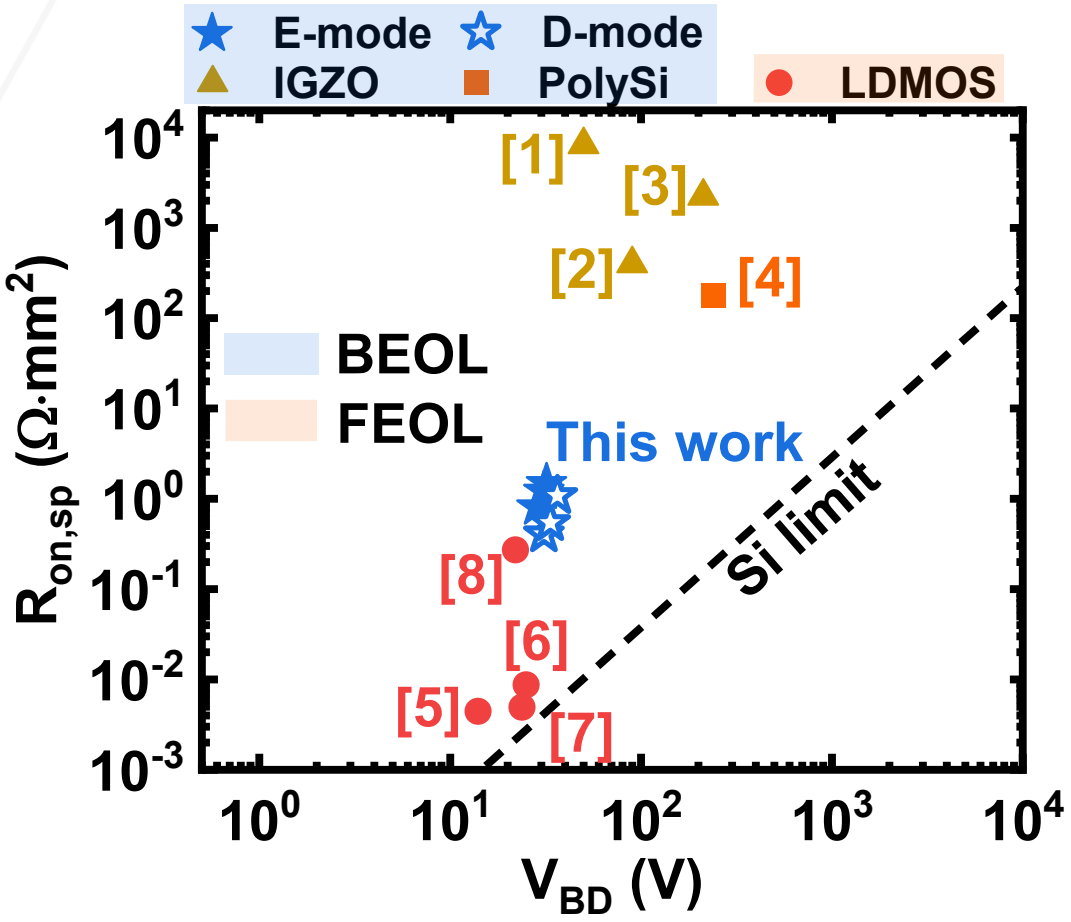
Benchmarking of BEOL Compatible Power FETs



- IWO power FETs show >1000x reduction in $R_{on,sp}$ compared with other BEOL-compatible power FETs.
- LDMOS with similar V_{BD} have lower $R_{on,sp}$, but this technology is BEOL incompatible.

[1] G. Yang, et al., TED 2021. [2] C. Park, et al., EDL 2021. [3] H. Huo, et al., Semicond Sci Tech 2021. [4] H.C. Cheng, et al., J. Electrochem. Soc. 2004. [5] P.Y. Huang, et al., ISPSD 2014. [6] H. Lin, et al., VLSI 2021. [7] S.Y. Chen, et al., TED 2021. [8] A. Houadef, et al., Eng. Proc. 2022.

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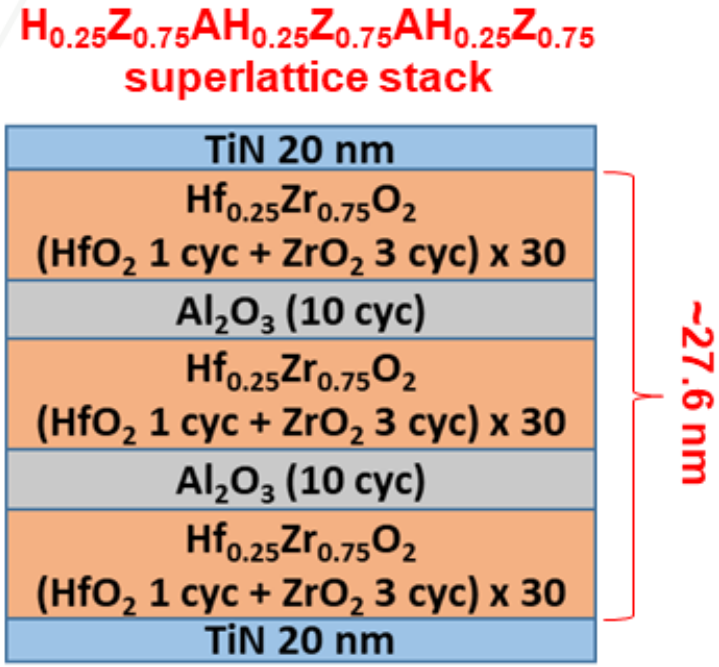
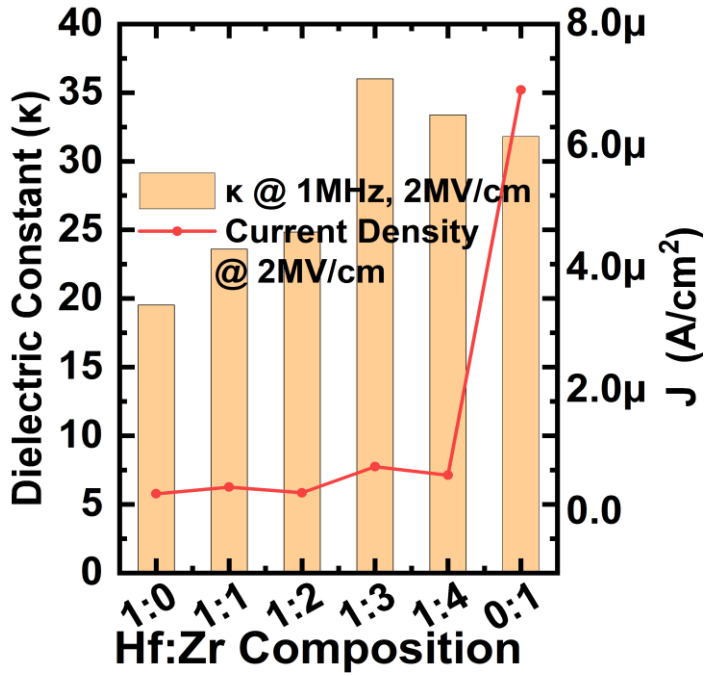
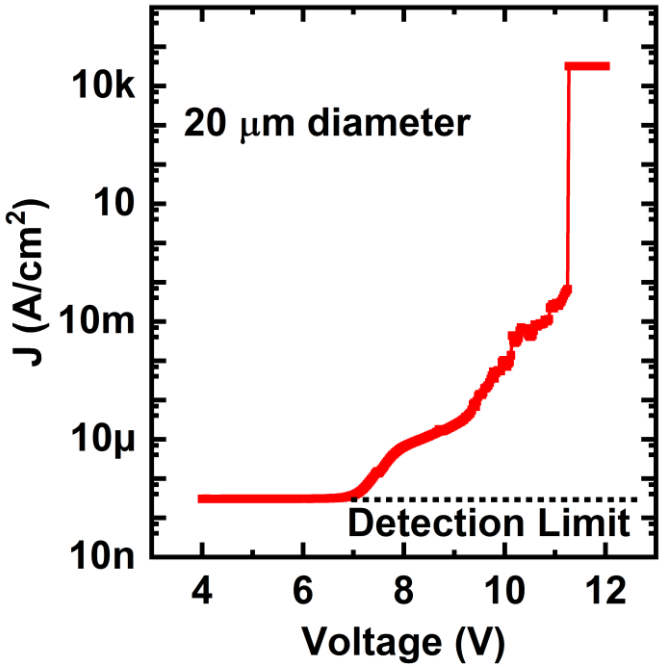
On-chip Superlattice MIM Capacitors







- $H_{0.25}Z_{0.75}O_2$ superlattice laminate: improve dielectric constant.
- Al_2O_3 interlayer: suppress m-phase formation and limit leakage in thicker superlattice stacks.

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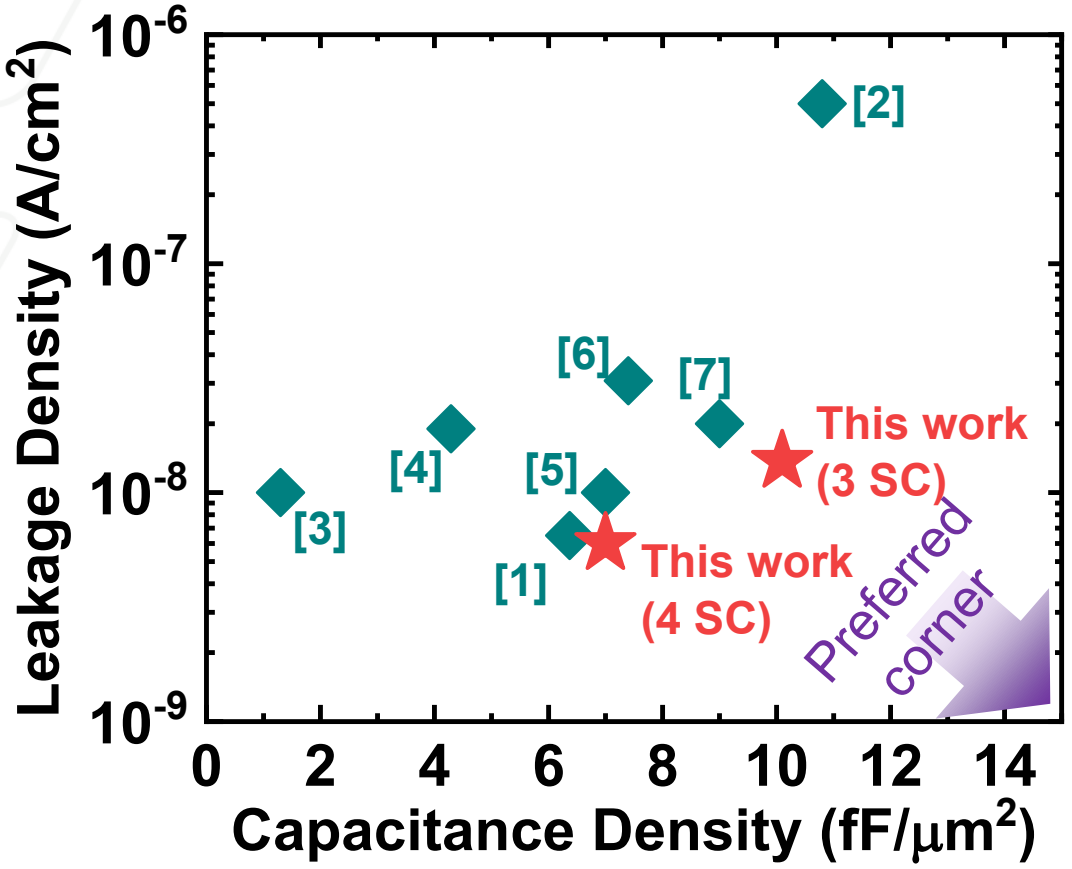
Benchmarking of On-Chip Planar Superlattice MIM Capacitors for High-Voltage Applications



- >34x reduction in leakage current with a high capacitance density (>10 fF/um^2).
- V_{BD} withstands the max. DC voltage stress for 2:1 step-down conversion from 12 V.

[1] H. Lin, et al., TVLSI 2022. [2] C. Fang, et al., EDL 2019. [3] G, Hellings, et al., VLSI 2015. [4] W. S. Liao, et al. IEDM 2014. [5] J. Kim, IEEE 3DIC 2015. [6] Q. -X. Zhang, et al. EDL 2014. [7] L. Zhang, et al. EDL 2009.

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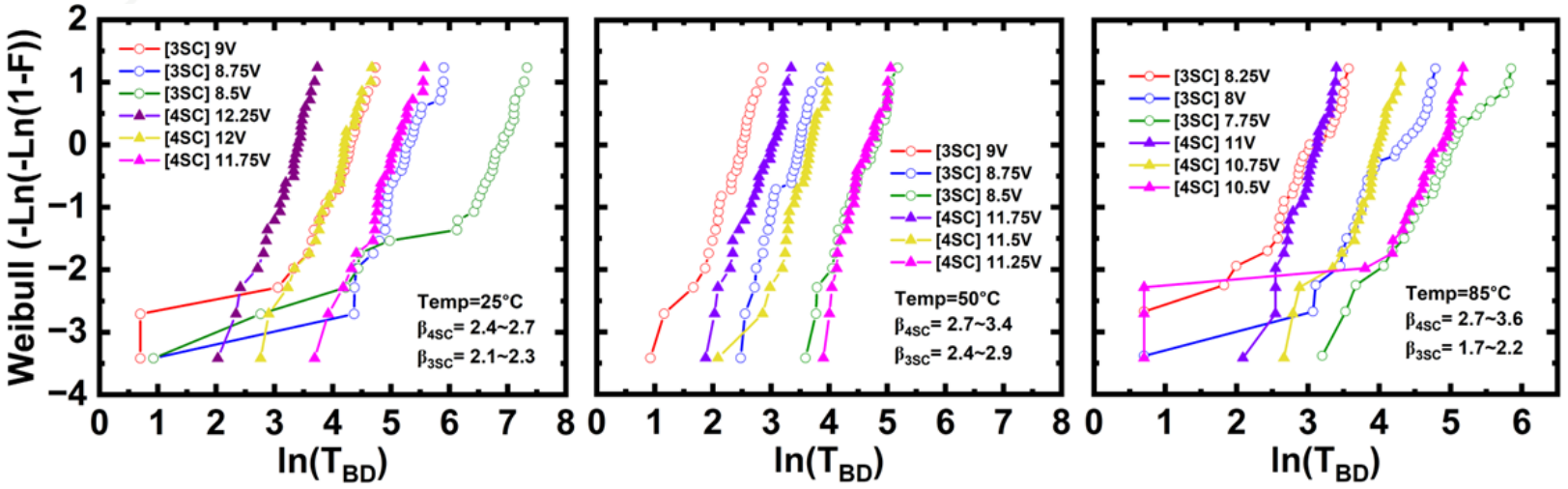
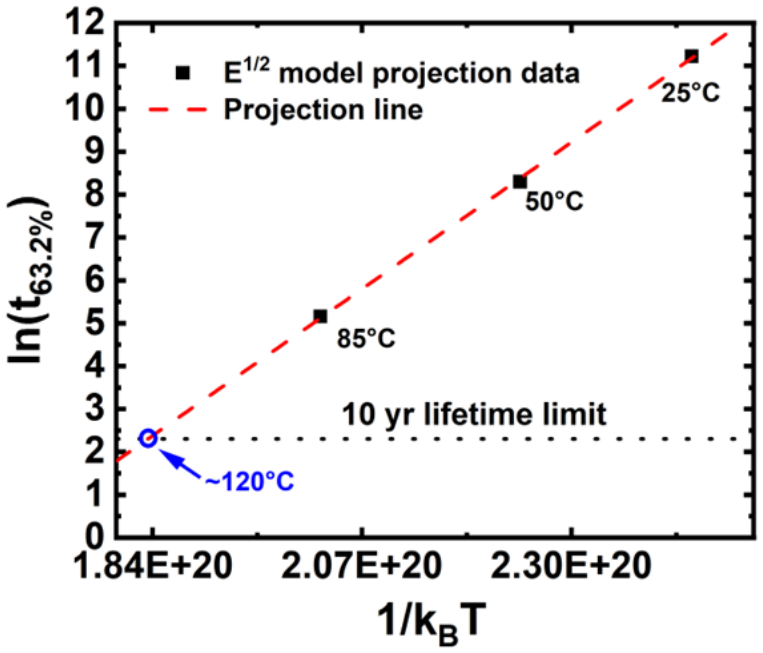
Reliability of High-Voltage On-Chip Superlattice MIM Capacitors

Weibull distribution at different temps.



Lifetime projection



- Poole-Frenkel conduction ($\ln(J) \propto \sqrt{E}$) dominates at 6 V.
- Projected lifetime of ~10 years at 6 V, 120°C ensures reliable on-chip voltage conversion from 12 V to 6 V.

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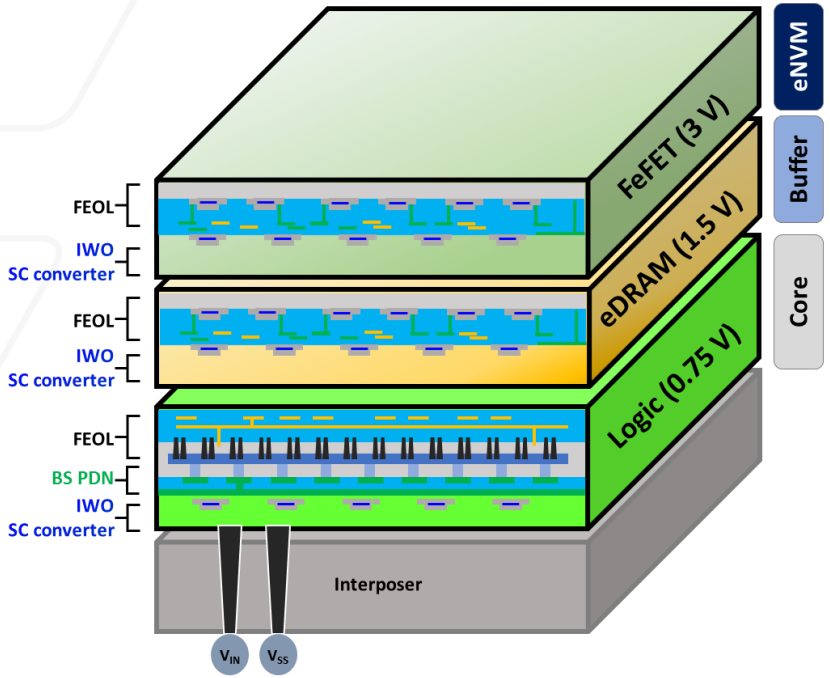
H3D Integrated Transformer Accelerator using On-Chip SC DC-DC Converters



Tier	FeFET	eDRAM	Logic
Application	Weight memory	Global buffer	self-attention & other kernel computing
Technology Node	22 nm	7 nm	2 nm
Device	IWO	IWO	CMOS
Supply voltage	3 V	1.5 V	0.75 V
Area	810.8 mm^2	817.9 mm^2	*719.2 mm^2
Bonding	Face-down	Face-down	Face-up
BEOL Power delivery	Front-side	Front-side	Back-side
Power density	1 mW/mm^2	4 mW/mm^2	*137.8 mW/mm^2
Capacity	8 GB	16 GB	-

- On-chip SC DC-DC converters are used to efficiently convert input voltage at the interposer level to the lower supply voltage domains required in each tier.

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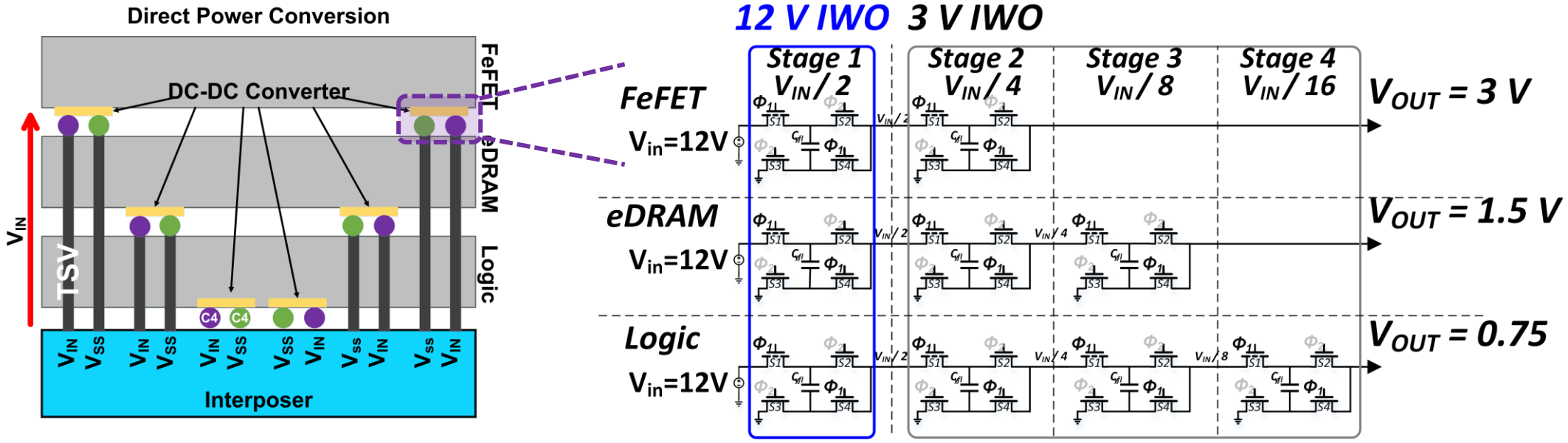
Multi-Stage On-Chip SC DC-DC Converters



- Input voltage directly delivered from the interposer to each tier in parallel.
- In each tier, cascaded unit SC DC-DC converters provide the desired supply voltages by multi-stage conversion.

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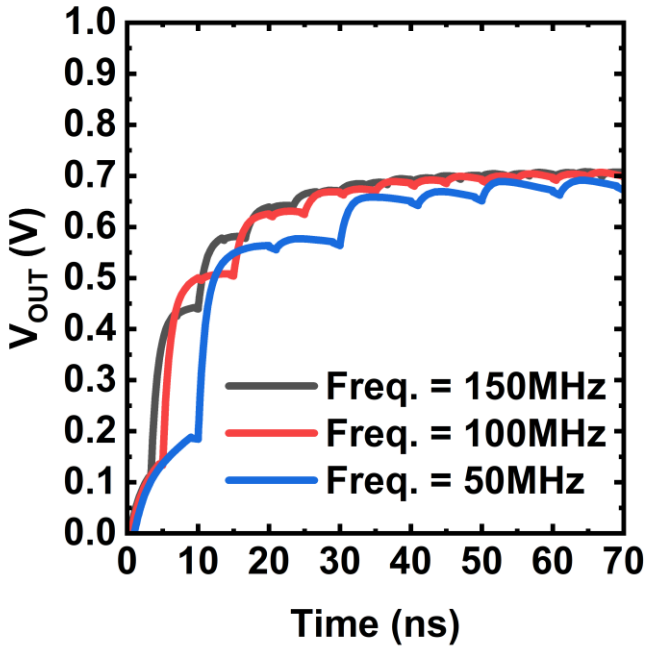
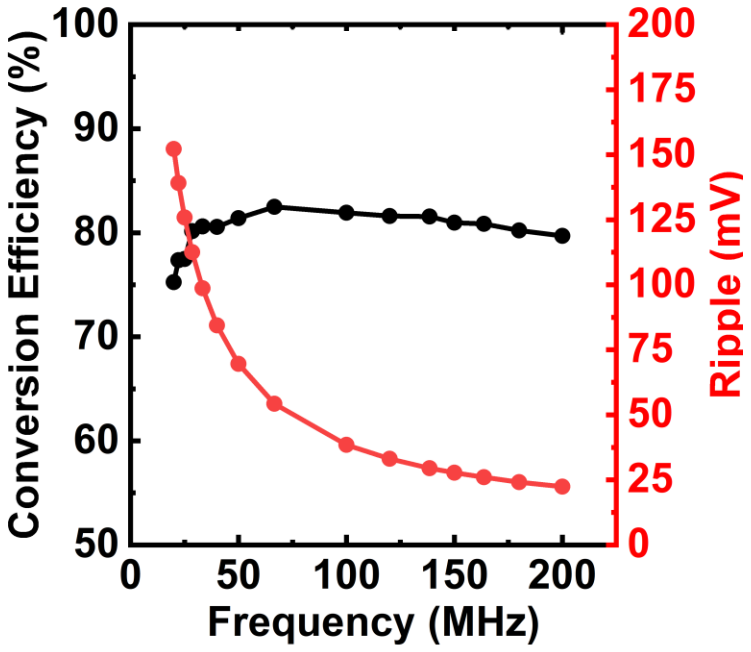
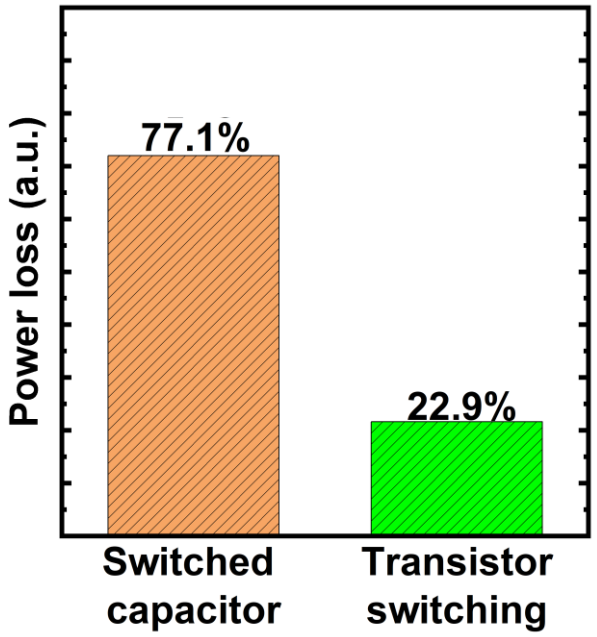
SPICE Simulation on Voltage Conversion







- The converters achieve ~83% efficiency (with a reasonable voltage ripple of 38 mV).
- Intrinsic loss is 3.4x higher than switching loss .

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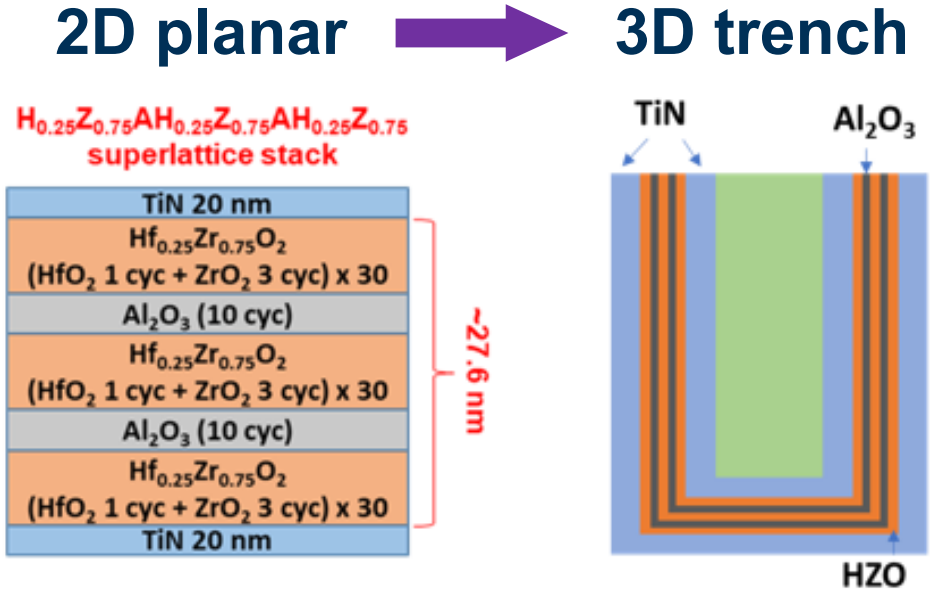
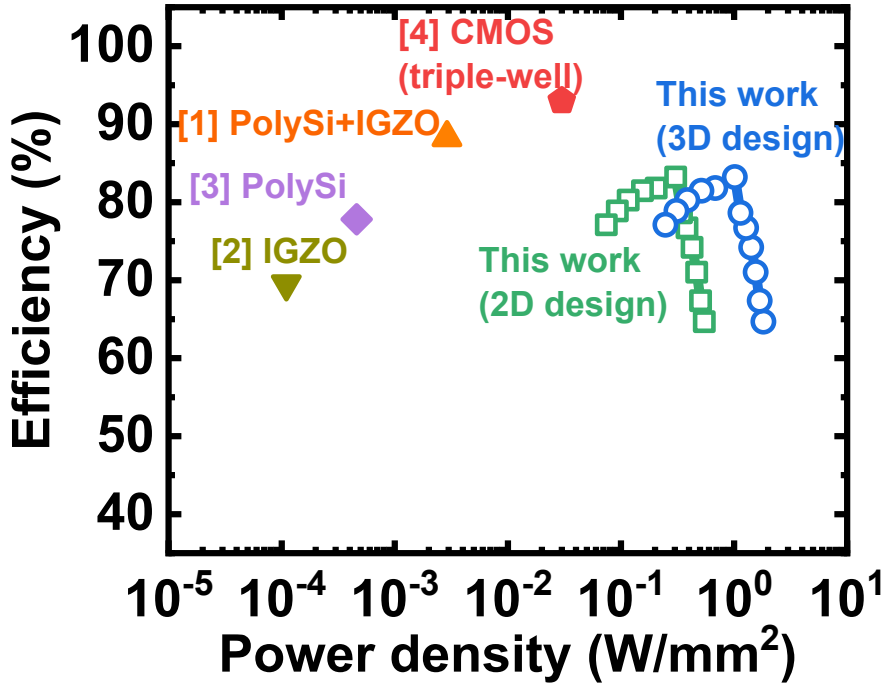
Design Optimization and Benchmarking





- Transition from 2D planar to 3D trench flying capacitors shows 3.3× increase in power density.
- Potentially competitive against SOTA FEOL-compatible technologies.

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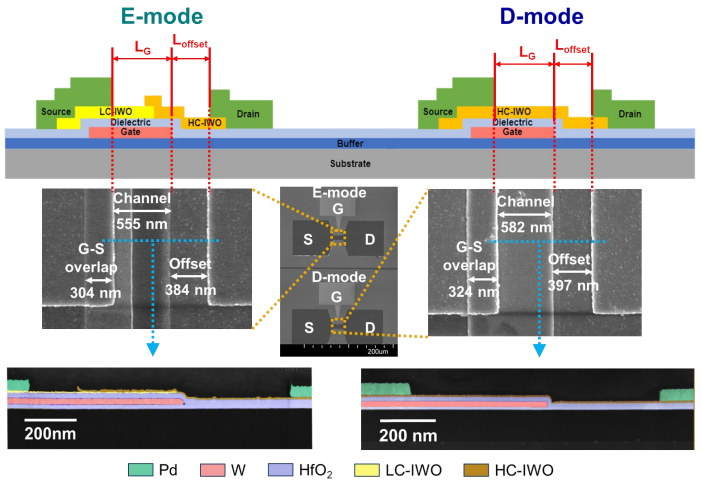
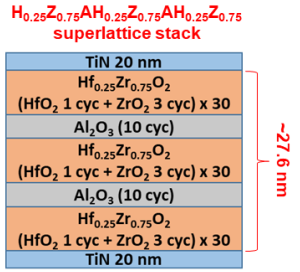
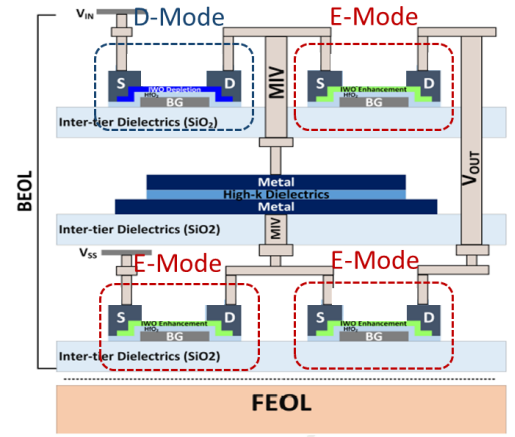
Summary

- Demonstrated the BEOL-compatible IWO power FETs with a drain V_{BD} of >12 V and a f_T of 192 MHz.
- Developed both E- and D-mode IWO power FETs, which could be co-integrated on the same chip.
- Demonstrated high-density high-voltage on-chip superlattice MIM capacitors with a projected lifetime of ~10 years at 120℃ and 6 V.
- Analyzed the performance of on-chip SC DC-DC converters showcasing a high efficiency of ~83% for H3D integrated transformer accelerators.







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Center for Heterogeneous Integration of Micro Electronic Systems

Thank you all for your attention

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