Back-Channel-Etched Oxide TFTs with Hybrid-Phase Microstructural ITO-Stabilized ZnO Channels

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Abstract

In comparison to metal oxide thin-film transistors (TFTs) with etch-stop-layer (ESL) architecture, back-channel-etched (BCE) devices enable more cost-effective manufacturing and the miniaturization of device footprint. Through optimizing the over-etch ratio during molybdenum source/drain electrodes patterning, and carrying out annealing treatment prior to that, the BCE oxide TFTs with hybrid-phase microstructural ITO-stabilized ZnO channels were successfully fabricated. The enhancement-mode devices exhibited good electrical characteristics with a typical field-effect mobility of 23.4 $cm^2/V{\cdot}s$. Besides, the reliability against gate-bias stress was also examined. Such devices were demonstrated to be promising in the applications of next-generation displays with higher resolution and frame rate, but lower costs.

Author Keywords

Back-channel-etched, thin-film transistor, ITO-stabilized ZnO, hybrid-phase microstructure, over-etch ratio, annealing.

1. Introduction

Metal oxide (MO) semiconductors with reasonable electrical properties, low manufacturing costs as well as transparency in visible light have drawn plenty of attention as the channel layers of thin-film transistors (TFTs). Apart from materials' own advantages, it is also feasible to upgrade the current a-Si TFT production lines, and forward towards MO-TFT-based panel manufacturing with less investments. This is thanks to the similar device architecture between these two types of TFTs. However, MO channels are not as insensitive to the following fabrication processes as a-Si. Thus, an additional etch-stop layer (ESL) was usually introduced to protect MO channel layer at the early R&D stage of MO TFTs. Although the electrical performance and reliability of devices can be guaranteed, it boosts the manufacturing costs, and also limits the miniaturization of device footprint for higher resolution displays considering the extra misalignment margin required in photolithography [1]-[3]. Therefore, the achievement of high-performance MO TFTs with back-channel-etched (BCE) structure is always highly demanded.

Many related efforts have been reported these years, most of which are concentered in a-IGZO channel layers. However, with the increase of pixel amount (≥8k×4k) and frame rate (≥120Hz) in next-generation displays, it is hard to ensure the mobility sufficiency in a-IGZO TFTs (~10cm^2/Vs) [4]. Although the optimization of circuit design or signal scanning scheme can more or less deal with the issue, the most fundamental solution is to replace a-IGZO layer by other potential MO materials with higher carrier mobility, such as InZnO [2] and InSnZnO [5][6]. Recently, our group also proposed a competitive kind of MO channel candidate, which was named as ITO-stabilized ZnO and owned hybrid-phase microstructure. It was demonstrated that the deposited thin films exhibited boosted carrier mobility, comparable spatial uniformity, and robust ambient stability in comparison with a-IGZO [7]-[10].

In this work, the oxide BCE TFTs with hybrid-phase microstructural ITO-stabilized ZnO channels were successfully fabricated. Mo source/drain (S/D) electrodes were patterned using hydrogen peroxide (H_2O_2)-based wet etchant. The influence of over-etch ratio and prior annealing treatment on channel layers and devices were investigated. Based on the optimal treatments above, the corresponding devices presented high electrical characteristics. The reliability of devices against gate-bias stress was also examined at last.

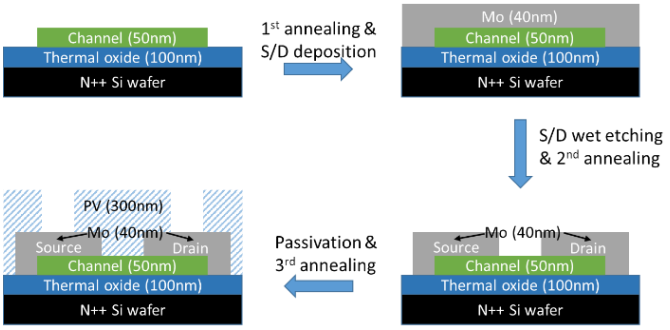

Figure 1. The entire fabrication process flow of BCE oxide TFTs with hybrid-phase microstructural ITO-stabilized ZnO channels.

2. Experimental

In order to study the influence of Mo wet etching on channel bulk as well as back-channel interface between channel and passivation layer, the entire fabrication processes (Figure 1) initiated on 4-inch Si/SiO_2 wafers. The heavily n-type doped Si substrate and the coated 100-nm-thick thermally grown SiO_2 layer were regarded as the gate electrode and gate dielectric of TFT, respectively. Thus, when analyzing results, we could less consider gate dielectric and front-channel interface between gate dielectric and channel layer, the high quality of which has been verified [8]. Then, 50-nm-thick channel layer was deposited via magnetron co-sputtering the polycrystalline ITO target and ZnO target. The optimal deposition conditions were described elsewhere [8]. After channel island patterning in diluted hydrofluoric (HF) acid, part of samples were annealed in air for 2h at the temperature of 300°C (the 1st annealing), and the rest were not. Next, all the samples were covered by 40-nm-thick Mo

layer using sputtering. After photolithography and hard baking, Mo layer was patterning into S/D electrodes in wet etchant (KANTO-PPC, MAE 295 series) at 35°C, and the over-etch ratio varied from 20% to 80%. All the devices were further annealed (the 2nd annealing) to repair the back-channel damages caused by the previous wet etching process. Afterwards, 300-nm-thick PECVD-SiO_2 was deposited on the top of devices as passivation layer, followed by contact hole opening using reactive ion etching (RIE). Finally, the 3rd annealing treatment was conducted again to do dehydrogenation and electrically activate devices. The electrical characteristics of TFTs were measured in the probe station using a semiconductor parameter analyzer (Agilent 4156C).

3. Results and Discussion

3.1 The influence of over-etch ratio

The Mo wet etchant is mainly composed of H_2O_2, amino additive and water. Theoretically, the relevant mechanism for Mo wet etching follows the reaction formulas as follows [11]:

$$Mo + 2H_2O_2 \rightarrow MoO_2 + 2H_2O \quad (1)$$

$$MoO_2 + H_2O_2 \rightarrow MoO_4^{2-} + 2H^+ \quad (2)$$

It can be found that Mo wet etching in H_2O_2-based etchant includes at least two steps in fact. Herein we assume the as-etched time corresponds to the total time consumed when metal luster completely disappears. However, this moment does not represent the end of wet etching, and there are still metal and metal oxide residues remaining on back-channel surface according to Equation 1. Therefore, over-etch treatment is necessary for residue removal. Otherwise, the electrical characteristics and reliability of devices will be degraded due to the etching residues, which behave as acceptor-like states at back-channel interface [2][12]. Therefore, it is worthy of investigating the influence of different over-etch ratio on devices.

Table 1. Thickness of the equivalent etching residues with different over-etch ratio in Mo wet etching process

Over-etch time (s)	30	60	90	120
Over-etch ratio (%)	20	40	60	80
Equivalent SiO_2 thickness (nm)	3.9	1.2	0.8	0.7

In this work, the as-etched time for 40-nm-thick Mo layer in 35°C etchant is around 150s, and the over-etch time varies from 30s, 60s and 90s to 120s, corresponding to the over-etch ratio of 20%, 40%, 60% and 80%, respectively. It should be noted that all the samples discussed in Section 3.1 have been treated by the 1st annealing process before Mo wet etching. With the measurement of Nanospec reflectometer (Nanometrics), the remaining thickness of etching residue could be approximately indicated by the equivalent thickness of SiO_2, which are listed in Table 1. It is found that the etching residues are almost eliminated with little thickness variation when the over-etch ratio rises from 40% to 60%. However, it does not mean that the over-etch time should be as long as possible. Figure 2 show the photo-micrographs of channels with an over-etch ratio of 60% and 80%. There is obvious corrosion phenomenon in the latter channel regions. This is because the reactions to dissolve molybdenum oxide residues will also release H^+ ions (Equation 2) at the same time. The more exposure to the wet etchant, the more portion of back-channel surface will be eroded, in spite of the existence of pH-value stabilizer.

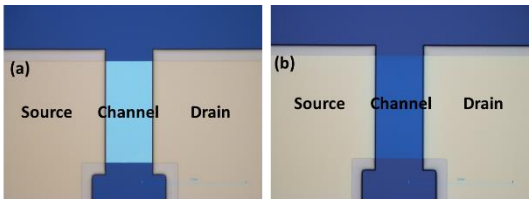

Figure 2. The photo-micrographs of channel regions in BCE oxide TFTs with an over-etch ratio of (a) 60% and (b) 80%.

Figure 3 exhibit the transfer curves of BCE oxide devices with different over-etch ratio. The tested TFTs are distributed across 4-inch substrates from edge to center position, so their spatially electrical uniformity can be examined as well. As observed, the electrical behavior of devices gets increasingly uniform when the over-etch ratio increases from 20% to 60%. In particular, the transfer curves of 9 TFTs with an over-etch ratio of 60% are almost overlapped; meanwhile, the jitter phenomenon in subthreshold region, which is related to the trap states in channel bulk, also disappears. These are owing to the nearly complete removal of etching residues, so that the back-channel conditions vary little from device to device. Besides, there is slight reduction of on-state current. The presumable reason is attributed to the increase of actual channel length, which is caused by gradually severe lateral etching with the extension of over-etch time. Furthermore, when the over-etch ratio climbs to 80%, the devices are found to be deteriorated significantly. This is consistent with the channel corrosion that observed in Figure 2(b). Above all, the optimal over-etch ratio should be between 40% and 60%, then the high-performance and uniform BCE oxide devices across large area could be confirmed.

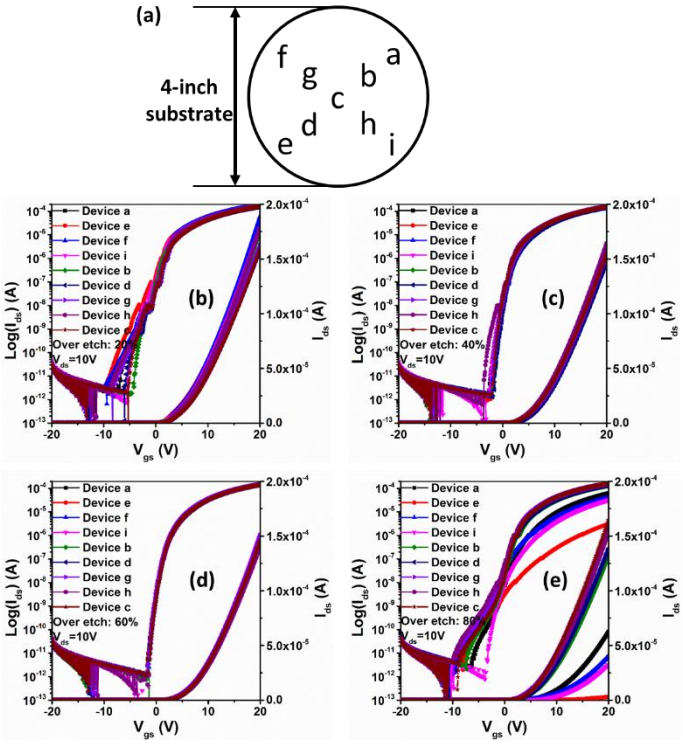

Figure 3. (a) The position schematic of tested devices across 4-inch substrate. The transfer curves of BCE oxide TFTs with an over-etch ratio of (b) 20%, (c) 40%, (d) 60%

and (e) 80%.

3.2 The influence of 1st annealing treatment prior to Mo wet etching

As mentioned, excess over-etch treatment is harmful to TFTs due to channel corrosion by H^+ ions in wet etchant. However, in order to completely eliminate the etching residues, the back-channel surface will encounter the wet etchant inevitably. In such circumstances, it is necessary to reduce the accompanied adverse impact as much as possible. One of efficient solutions is to strengthen the MO channel layer before Mo layer deposition, namely the 1st annealing treatment described in Section 2 above. Thus, the quality/density of channel layer can be improved, and its chemical resistivity to the following Mo wet etchant is also enhanced. According to our tests, the etching rate for as-deposited channel layer is as fast as about 17.3nm/min, which is comparable to that of Mo layer (~16nm/min). On the contrary, the etching rate for channel layer after thermal annealing becomes more than 4 times slower (<4nm/min). Figure 4(a) is the photo-micrograph of unannealed channel region with an over-etch ratio of 60%. Compared with Figure 2(a), the channel layer is obviously damaged without prior annealing enhancement, and the corresponding devices also present much more inferior electrical performance (Figure 4(b)). Therefore, it is evident that the 1st annealing treatment is highly essential, which could enlarge the effective range of over-etch ratio in Mo wet etching process.

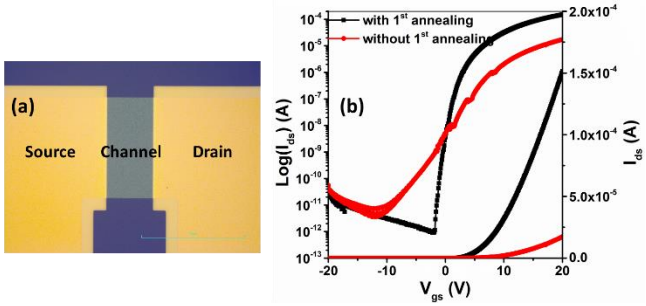

Figure 4. (a) The photo-micrograph of unannealed channel region in BCE oxide TFTs with an over-etch ratio of 60%. (b) The transfer curves of BCE oxide TFTs without the 1st annealing treatment, in comparison with that of devices with the 1st annealing treatment.

3.2 The electrical characteristics and reliability of the optimal BCE oxide TFTs with hybrid-phase microstructural ITO-stabilized ZnO channels

Through optimizing the over-etch ratio during Mo S/D electrodes patterning, and carrying out thermal annealing treatment prior to that, the BCE TFTs with hybrid-phase microstructural ITO-stabilized ZnO channels can be fabricated with good electrical performance. The corresponding transfer and output curves of devices are plotted in Figure 5. Such devices exhibited a typical field-effect mobility of 23.4 $cm^2/V{\cdot}s$, threshold voltage of 0.7 V, on-off ratio of over 10^8, and subthreshold swing of 0.289 V/decade. Compared with the similar TFTs but employing the lift-off S/D electrodes [8], the BCE devices herein show worse subthreshold swing and on-off ratio (or higher off-state current). Since the main difference between these two types of devices is the patterning technique of S/D electrodes, the performance degradation is believed to origin from the back-channel damages and the etching residues, as reported in some references [2][12]. Therefore, further optimization from other aspects needs to be conducted in the future. According to the output curves, there is little current crowding effect observed at low drain voltage. This indicates the good ohmic contacts between S/D electrodes and channel layer.

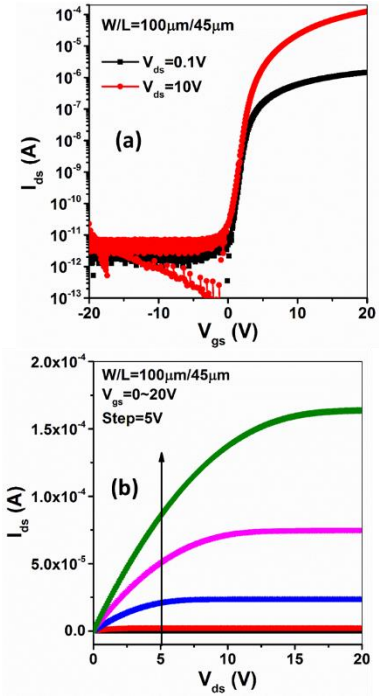

Figure 5. (a) Transfer curves and (b) output curves of the optimal BCE oxide TFTs with hybrid-phase microstructural ITO-stabilized ZnO channels.

Moreover, the basic reliability of devices against gate-bias stress was examined, as shown in Figure 6. The V_{ds} is kept at 5 V, and the applied V_{gs} for PBS and NBS is set to (V_{th}+20) V and (V_{th}-20) V, respectively, for 10 000 s. In the subthreshold region of both cases, there is no stretch-out phenomenon, indicating few defects are generated during the stress tests. However, the contact between S/D electrodes and channel layer deteriorates at the same time, and results in on-state current reduction. Besides, there is little threshold voltage shift in PBS case, whereas threshold voltage negatively shifts about 1V in NBS case. It reveals that there may exist electron traps at back-channel interface between channel and passivation layer. When negative gate bias stress is applied, electrons will move towards back-channel interface and get trapped. These trapped electrons can build a negative potential at back channel and repel the rest electrons towards front-channel interface, leading to a negative shift of threshold voltage. In this way, further improvement work is required to cancel these electron traps.

4. Conclusion

In this work, the BCE oxide TFTs with hybrid-phase microstructural ITO-stabilized ZnO channels were successfully fabricated. Through annealing channel layer before Mo S/D wet etching process, the chemical resistivity of channel layer to H_2O_2-based wet etchant could be enhanced significantly with less back-channel damages. Besides, the optimal over-etch ratio was found in the range between 40% and 60%, where the etching residues could be almost removed without excess channel corrosion. The BCE devices after above optimization exhibited good electrical performance with a typical field-effect mobility of 23.4 $cm^2/V{\cdot}s$

and a threshold voltage of 0.7 V. The results were promising in the applications of next-generation cost-effective displays with higher resolution and frame rate.

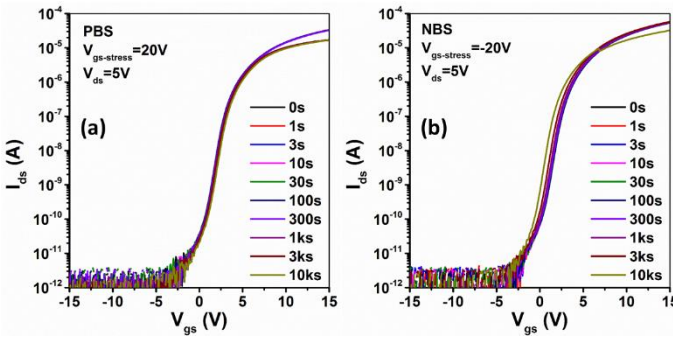

Figure 6. Transfer curve variation of the optimal BCE oxide TFTs with hybrid-phase microstructural ITO-stabilized ZnO channels under (a) PBS and (b) NBS tests for 10 000 s.

5. Acknowledgements

This work was supported in part the Research Grants Council, Hong Kong Government through the Theme-Based Research Project under Grant No. T23-713/11-1, in part by the Partner State Key Laboratory on Advanced Displays and Optoelectronics Technologies under Grant ITC-PSKL12EG02, in part by National Natural Science Foundation of China under Grant 61604057, and in part by Science and Technology Program of Guangdong Province under Grant 2017A010101010. The authors thank the facility support of the Nanosystem Fabrication Facility (NFF-HKUST), Materials Characterization and Preparations Facility (MCPF-HKUST), and the Center for Nanoscale Characterization and Devices (CNCD-WNLO-HUST).

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